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Temperature sensitivity analysis of polarity controlled electrostatically doped tunnel field-effect transistor

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ABSTRACT

The conventional tunnel field-effect transistors (TFETs) have shown potential to scale down in sub-22 nm regime due to its lower sub-threshold slope and robustness against short-channel effects (SCEs), however, sensitivity towards temperature variation is a major concern. Therefore, for the first time, we investigate temperature sensitivity analysis of a polarity controlled electrostatically doped tunnel field-effect transistor (ED-TFET). Different performance metrics and analog/RF figure-of-merits were considered and compared for both devices, and simulations were performed using Silvaco ATLAS device tool. We found that the variation in ON-state current in ED-TFET is almost temperature independent due to electrostatically doped mechanism, while, it increases in conventional TFET at higher temperature. Above room temperature, the variation in I_{ON}, I_{OFF}, and SS sensitivity in ED-TFET are only 0.11%/K, 2.21%/K, and 0.63%/K, while, in conventional TFET the variations are 0.43%/K, 2.99%/K, and 0.71%/K, respectively. However, below room temperature, the variation in ED-TFET I_{ON} is 0.195%/K compared to 0.27%/K of conventional TFET. Moreover, it is analysed that the incomplete ionization effect in conventional TFET severely affects the drive current and the threshold voltage, while, ED-TFET remains unaffected. Hence, the proposed ED-TFET is less sensitive towards temperature variation and can be used for cryogenics as well as for high temperature applications.

1. Introduction

As the CMOS scaling approaches sub-22 nm regime, the Moore's Law and its scaling principle is dying because it faces enormous challenge at this scaled dimension, such as, reduced gate controllability, exponential increase in leakage power, and short channel effects (SCEs) [1]. Therefore, It is indeed need of today's era in semiconductor world to find a numerous alternatives over CMOS technology. In various possible devices, tunnel field effect transistors (TFETs) have attracted huge attention from the device and research community due to its potential advantage of sub-threshold slope (SS) less than 60 mV/dec at 300 K, and low leakage current [2]–[4]. However, dopant fluctuations of highly doped source and drain regions in Ref. [5] at aggressively scaled device dimensions also imposes several issues for its thermal budget. Moreover, TFETs reported in Refs. [4,6], are more sensitive towards temperature variation, as temperature causes several issues on device operation because it influences device electrical parameters, such as I_{ON}, I_{OFF}, SS, and V_{TH}.

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Therefore, to address the sensitivity towards temperature variation, we investigate temperature sensitivity analysis of a polarity controlled electrostatically doped TFET. In this work, the effect of temperature on performance metrics, such as, transfer characteristics, carrier concentration profile, ON-state current, threshold voltage (V_{TH}), and total gate capacitance (C_{gg}) are analysed for the proposed ED-TFET over conventional TFET. Next, the effect of temperature on analog/RF figure-of-merits, such as, transconductance (g_m), cut-off frequency (f_T), and transconductance generation factor (TGF) have also been investigated for conventional and proposed device. The effect of incomplete ionization have also been considered to analyse the performance metrics at cryogenic temperatures [7]. From ATLAS device simulations, the proposed device shows less sensitivity in terms of I_{ON}, I_{OFF}, SS, g_m, C_{gg}, f_T, and TGF with temperature variation.

The remaining parts of this paper are organized as follows: Section 2 incorporates the device schematic, analysis of device operating mechanism, parameters, and its simulation setup. Section 3 focuses on simulation results and discussion. Section 4 discusses the impact of temperature on analog/RF figure-of-merits. Finally, Section 5 concludes with some key findings.

2. Device schematic, design specification and simulation setup

Fig. 1(a–b) illustrate the cross-sectional view of conventional TFET and proposed ED-TFET. The design parameters used in simulation of the proposed device are shown in Table 1. In order to exemplify the primary requisite of ED-TFET, the basic approach is used to convert n^+-n^+-n^+, (drain, channel and source) into n^+-i-p^+ (Tunnel FET). In proposed structure, metal work function of polarity gate (PG) is same as controlling gate (CG), which is used to make the layer beneath PG and CG of intrinsic nature. Next, by applying appropriate negative voltage at the polarity gate ($V_{PG} = -1.2$ V), the holes (in the order of 10^{19} cm^{-3}) are induced underneath the undoped PG region. Interestingly, it is seen that n^+-i-p^+ like structure is made on an undoped Si-nanowire even without any metallurgical doping using the electrostatic doping and the concentration profile has followed the same trend as like conventional TFET [4], and does not change significantly along the lateral direction. However, S/D contact is made using nickel silicide (NiSi) with a barrier height of 0.45 eV [8,15]. In addition, a spacer thickness (L_{gap},S) of 5 nm is used between CG and PG towards the source side.

The simulations are performed by using 2D Silvaco ATLAS device simulator [9]. Physical process inside the device is mainly accounted by incorporating TCAD model. For TFETs, the most important model is band-to-band tunneling (BTBT) model [9]. In local and non-local models, a suitable option can be made between both in which the first one uses simple mathematical equations, where electric field is an important parameter. On the other hand, second depends on the band diagrams calculated along cross-sections through the device [9]. In ED-TFET, the non-local BTBT model were considered for simulations which uses WKB approach for measuring the tunneling probability using electron hole wave-vector throughout the tunneling path. However, a band gap narrowing model with some other physical models such as Augur, SRH, field dependent mobility and Fermi-Dirac statistics are also considered in the simulation. The mesh has been refined very carefully in the tunneling zone to assist the accuracy and numerical efficiency. For better accuracy, Schenk's trap-assisted tunneling (TAT) models given

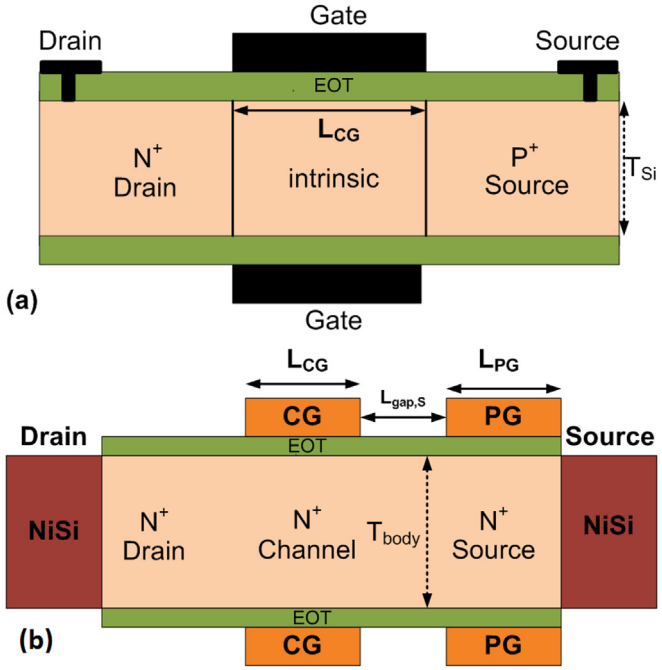

Fig. 1. Cross-sectional view of (a) conventional TFET [4], and (b) proposed ED-TFET.