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Investigation of InP/$In_{0.65}Ga_{0.35}As$ metamorphic p-channel doped-channel field-effect transistor

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ABSTRACT

In this article, the device mechanism and characteristics of InP/InGaAs metamorphic p-channel field-effect transistor (FET), which has a high indium mole fraction of InGaAs channel, grown on the GaAs substrate is demonstrated. The device was fabricated on the top of the $In_xGa_{1-x}P$ graded metamorphic buffer layer, and the $In_{0.65}Ga_{0.35}As$ pseudomorphic channel was employed to elevate the transistor performance. For the p-type FET, due to the considerably large valence band discontinuity at InP/$In_{0.65}Ga_{0.35}As$ heterojunction and a relatively thin as well as heavily doped pseudomorphic $In_{0.65}Ga_{0.35}As$ channel between two undoped InP layers, a maximum extrinsic transconductance of 27.3 mS/mm and a maximum saturation current density of −54.3 mA/mm are obtained. Consequently, the studied metamorphic FET is suitable for the development in signal amplification, integrated circuits, and low supply-voltage complementary logic inverters.

1. Introduction

Due to the high electron mobility and saturation velocity, InP/InGaAs heterostructure field-effect transistors (HFETs) are emerging as key devices for high-speed electronic and circuit applications [1–3]. In particular, complementary HFETs are promising devices for logic circuit applications because of the low standby power consumption, excellent threshold-voltage uniformity, and large noise margin, etc. [4]. However, as compared with the n-channel devices, the performance of complementary HFETs is severely limited by the p-channel transistors for the low out current and transconductance, which is originated from the relatively small hole mobility [5–7]. Though the InP/InGaAs HFETs possess some unique advantages, InP substrates are expensive, fragile, and easily broken during the fabricated process than the GaAs-based transistors. Recently, InP-based metamorphic transistors grown on the low-cost GaAs substrates have been well investigated [8–10]. Herrick et al. depicted the power characteristics of metamorphic high electron mobility transistor (HEMT) [8]. In addition, the characteristics of $In_{0.42}Al_{0.58}As/In_{0.46}Ga_{0.54}As$ metamorphic HEMTs with double and single δ-doped structures were studied by Liu et al. [9].

With regard to the metamorphic transistors, the $In_xGa_{1-x}P$ graded buffer layer of the metamorphic HBTs, varying from $In_{0.52}Ga_{0.48}P$ to InP, could provide better thermal properties resulting from a much smaller thermal resistance as compared to the widely used InAlAs metamorphic buffer layer [11]. Furthermore, unlike the GaAs-based transistors, the indium mole fraction and thickness of the InGaAs channel layer can be further extended because of the small lattice constant mismatch with InP material layer. In this article, an InP/$In_{0.65}Ga_{0.35}As$ metamorphic doped-channel FET (DCFET) fabricated on GaAs

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substrate is reported. As concerning to the DCFETs, a large energy-gap and undoped material layer acts as a Schottky barrier to increase gate voltage swing. Also, the drain current could be enhanced by the use of a thin as well as heavily doped channel [12–14]. The large gate voltage swing could improve the device linearity and reduce the higher order harmonic terms in linear amplifier applications [12]. By the use of an $In_{0.65}Ga_{0.35}As$ pseudomorphic channel layer, the p-channel FET exhibits large gate forward operation voltage, drain current, and transconductance, simultaneously.

2. Experiments

The studied InP/InGaAs metamorphic DCFET were grown on an (100) oriented semi-insulating GaAs substrate by molecular beam epitaxy (MBE) system. The epitaxial structures consisted of a 1.5 μm undoped and linearly graded $In_xGa_{1-x}P$ (x: 0.52 → 1) metamorphic buffer layer, a 0.15 μm InP undoped layer, a 100 Å $n^+ = 1 \times 10^{18}$ cm^{-3} $In_{0.65}Ga_{0.35}As$ n-channel layer, a 100 Å InP undoped layer, a 300 Å i-$In_{0.65}Ga_{0.35}As$ layer, a 200 Å InP undoped layer, a 100 $p^+ = 3 \times 10^{18}$ cm^{-3} $In_{0.65}Ga_{0.35}As$ p-channel layer, an 80 InP undoped gate layer, and a 300 $p^+ = 1 \times 10^{19}$ cm^{-3} $In_{0.53}Ga_{0.47}As$ cap layer. The growth of the metamorphic buffer layer mainly used the method of the reference [11]. A sheet carrier density of 3.5×10^{12} cm^{-2} and hole mobility of 335 cm^2/V-s were obtained from Hall measurement. Drain and source ohmic contacts were formed by alloying the evaporated AuGeNi metal at 400 °C for 30 s. Sequentially, the p^+-InGaAs cap layer was recessed, and the gate metal Au was deposited on the InP gate layer. Before the gate metal was deposited, the drain-to-source (D-S) resistance was of 28 Ω/mm. The schematic cross section of the device is shown in Fig. 1. In the device, the gate dimension and the D-S spacing were 1×100 μm^2 and 3 μm, respectively. As to the stacked structure, the p-channel field-effect transistor was stacked on the top of the n-channel device grown on the $In_xGa_{1-x}P$ metamorphic buffer layer. This article mainly focuses the p-channel device, and the characteristics of the n-channel device will be discussed in further.

3. Experimental results and discussion

Fig. 2 illustrates the corresponding band diagram of the p-channel device at equilibrium. The gate potential barrier for holes is enough high by the relatively large valence band discontinuity (ΔEv ~ 0.43 eV) at InP/$In_{0.65}Ga_{0.35}As$ heterojunction. The high gate potential barrier could prevent the hole injection from channel into gate and increase the gate forward voltage and reduce gate leakage current. Furthermore, the $In_{0.65}Ga_{0.35}As$ p-channel layer is entirely depleted at equilibrium, attributed to the considerably high barrier height of the Au/InP gate Schottky contact. Thus, the device will act as an enhancement-mode transistor. Generally, the hole mobility of p-type channel is relatively small. So, the InGaAs channel was heavily doped to enhance the output current.

The experimental D-S current-voltage characteristics of the p-channel device are depicted in Fig. 3. A maximum drain current of −54 mA/mm at $V_{GS} = -3$ V and $V_{DS} = -6$ V is observed. The large gate-to-source operation voltage can be attributed to (i) the considerable gate potential barrier and (ii) the large channel resistance and spacing series resistance absorbing the more part of the gate voltage due to the small hole mobility. As the gate operation voltage is more negative, the

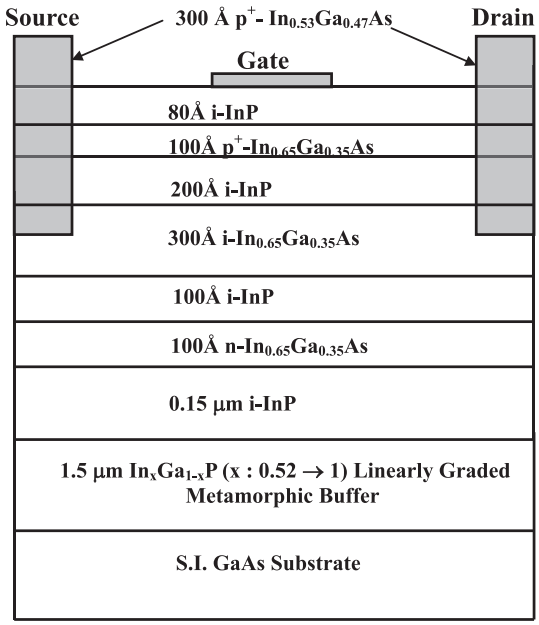

Fig. 1. Schematic cross section of the studied InP/InGaAs metamorphic p-channel field-effect transistor.