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A novel ultra steep dynamically reconfigurable electrostatically doped silicon nanowire Schottky Barrier FET

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ABSTRACT

In this paper, an ultra steep, symmetric and dynamically configurable, electrostatically doped silicon nanowire Schottky FET (E-SiNW-SB-FET) based on dopant-free technology is investigated. It achieves the ultra steep sub-threshold slope (SS) due to the cumulative effect of weak impact-ionization induced positive feedback and electrostatic modulation of Schottky barrier heights at both source and drain terminals. It consists of axial nanowire heterostructure (silicide-intrinsic silicon-silicide) with three independent all-around gates, two gates are polarity control gates for dynamically reconfiguring the device polarity by modulating the effective Schottky barrier heights and a control gate switches the device ON and OFF. The most interesting features of the proposed structure are simplified fabrication process as the state-of-the-art for ion implantation and high thermal budget no more required for annealing. It is highly immune to process variations, doping control issues and random dopant fluctuations (RDF) and there are no mobility degradation issues related to high doping. A calibrated 3-D TCAD simulation results exhibit the SS of 2 mV/dec for n-type E-SiNW-SB-FET and 9 mV/dec for p-type E-SiNW-SB-FET for about five decades of current. Further, it resolves all the reliability related issues of IMOS as hot electron effects are no more limiting our device performance. It offers significant drive current of the order of 10^{-5}-10^{-4} A and magnificently high I_{ON}/I_{OFF} ratio of ~10^{8} along with the inherent advantages of symmetric device structure for its circuit realization.

1. Introduction

Due to the various fundamental challenges at sub-22 nm CMOS scaling, M. Y. Vardi et al. “The Moore's Law & Sand Heap Paradox” [1]. It suggests that due to enormous detrimental effects at this scaled dimensions such as, reduced gate controllability resulting in short channel effects (SCEs), low drive current, sub-threshold leakage as a result of the non-scalability of supply voltage and exponentially increasing leakage power, it is difficult to sustain this law of scaling [2–4]. Hence, he concluded that “Moore's Law is Dying” [1]. Thus, in order to complement or replace the conventional CMOS, several charge based beyond CMOS device architectures such as impact ionization MOS (IMOS) [5,6] and tunnel FETs (TFETs) [7–9] are explored. These devices have fascinated researchers due to their ability to combat the fundamental “Boltzmann Tyranny” of conventional FETS. Hence, they have the potential to scale sub-threshold slope (SS) below 60 mV/dec at room temperature (300° K). This scalability of SS leads to the scalability of supply voltage as well. Further, steep SS is the most feasible solution to reduce the leakage current exponentially as, leakage current (I_{Leak}) is governed by

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$$I_{Leak} = I_D\Big|_{V_{GS}=V_{Th}}.10^{-\frac{V_{Th}}{SS}} \quad (1)$$

where, I_D is drive current, V_{GS} is applied gate-to-source voltage and V_{Th} denotes threshold voltage. Despite of these advantages these devices have major drawbacks as IMOS has high operating voltage and hot electron effects adversely affecting the device reliability [6]. In addition to this, both IMOS and TFET have asymmetric p-i-n structure restricting their circuit level realization in bidirectional current flow paths. TFET's low drive current is the major issue due to which it is still not matured enough to complement CMOS technology. Further, the inclusion of a lateral impact ionization region (I-region) involves the formidable lithography challenges related to the alignment error. These alignment errors, introduced during lithography also affects the device characteristics and reliability negatively [10]. Moreover, as the scaling prevails the ultra-steep doping profile is required for source/drain regions realization in p-i-n structure. As a result of complex fabrication process flow, the scalability of both of these asymmetric devices is detrimental to their electrical characteristics. Moreover, at such aggressively scaled device dimensions, dopant fluctuations [11,12] and dopant activation [13] of highly doped source and drain regions also leads to higher thermal budget. To combat these doping related issues, the electrostatic doping concept is explored for reconfigurable-FET (RFET), apart from the dopant-free nature it also exhibits dynamic reconfigurability, as RFETs can behave either as n or p-FET depending on the biases applied at various gates. It is also investigated experimentally [14–17]. Interestingly, same device can also act either as TFET or IMOS [18]. The concept of dual polarity and symmetric electrical characteristics is explored for its various aspects [19–25]. Still, they suffer from the fundamental thermodynamic limit (kT/q limit) of non-scalable SS.

Hence, to combine the dopant-free and symmetric nature with ultra steep SS behavior in single device structure, we investigate an ultra steep, symmetric, dynamically configurable (either as n-type or as p-type) silicon nanowire (SiNW) electrostatically doped Schottky barrier FET (E-SiNW-SB-FET). For the first time, we report ultra steep behavior for the reconfigurable SB-FET. It achieves the ultra steep SS due to the cumulative effect of weak impact-ionization induced positive feedback and electrostatic modulation of Schottky barrier heights at both source and drain terminals. It consists of axial nanowire heterostructure (silicide(source)-intrinsic silicon(channel)-silicide(drain)) having three independent all-around gates (TIGs) for dynamic configuration of Schottky barriers at both source and drain sides. Out of these three gates two gates are polarity control gates (PCGs), employed for dynamically reconfiguring the device polarity by modulating the effective Schottky barrier heights and a control gate (CG) is used for switching the device ON and OFF. To elucidate the potentials of proposed device and physics for device working mechanism in-detail, 3D-TCAD simulations are used. The most interesting features of the proposed structure is its ultra steep SS along with dynamic switching of device polarity and simplified fabrication process. It offers reduced the thermal budget of the device fabrication process, hence it facilitates its fabrication even on single crystal silicon-on-glass substrate by wafer scale epitaxy transfer [26,27]. It promotes the devices potential bio and opto compatibility [28]. TCAD simulation results exhibit the SS of 2 mV/dec for n-type E-SiNW-SB-FET and 9 mV/dec for p-type E-SiNW-SB-FET. All these device performance parameters are in accordance with the requirements of circuit realization along with symmetric structure. Hence, it demonstrates the immense potential as a futuristic low power fast switching symmetric transistors.

The remaining parts of this paper are organized as follows: Section 2 incorporates the device structure and simulation methodology. Section 3 focuses on comprehensive analysis of device operating mechanism, and simulation results and discussion. Finally, Section 4 concludes the key findings of this investigation.

2. Device structure and simulation set-up

The 3-D schematic, cross-sectional view and proposed circuit symbol of E-SiNW-SB-FET are shown in Fig. 1 (a)-(c) respectively. It consists of axial SiNW having background doping (N_{In}) as 1×10^{15} cm^{-3} of radius 10 nm and 170 nm long having heterostructure (silicide(source)-intrinsic silicon(channel)-silicide(drain)). Source and drain contacts are made up of nickel-silicide (NiSi) having barrier height (ϕ_B) of 0.45 eV. The orientation of SiNW is considered as ⟨110⟩. This axial SiNW also enabled future nano-circuits with added performance and functional values based on electrostatic doping, enhanced packaging density and excellent gate controllability due to the gate-all-around (GAA) structure. It has three independent all-around gates, PCGs dynamically reconfigure the device polarity by modulating the Schottky barrier heights and realizes two independent charge injection valves at both source and drain sides. CG turns the device ON and OFF by controlling the channel potential barriers for both n/p-type device. Structurally, both n/p-type devices are similar but they differ in their applied biases at the TIGs. The use of midgap Schottky-barrier source/drain contacts are the key enablers for this device concept to be efficiently functional, hence the affinity of SiNW is considered as χ_{SiNW} as 4.05 eV in order to maintain an identical mid-gap Schottky barrier height as 0.41 eV. Further, the midgap Schottky-barrier source and drain configuration promotes its robustness against high temperature environments and atomic abruptness of a Schottky-barrier compared to a conventional PN-junction shows immense potential for the long-term scalability of the devices. In conventional SB-FETs each type of transistor (n/p-type device) has its dedicated metal, corresponding to a specific metal-semiconductor work-function. This obstructs the on-the fly selectivity of the device polarity. Whereas, in the proposed E-SiNW-SB-FET device polarity is electrostatically controlled or voltage-selectable. This on-the fly selectivity of the device polarity facilitates the enhance device design in integrated circuits (ICs) and easy fabrication. Further, in order to isolate the impact of different applied biases