Superlattices and Microstructures 93 (2016) 138–143

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Sandwich double gate vertical tunneling field-effect transistor

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ARTICLE INFO

Article history:
Received 25 February 2016
Accepted 16 March 2016
Available online 19 March 2016

Keywords:
High-k dielectric material
Double gate (DG)
Vertical tunnel field effect transistor (VTFET)

ABSTRACT

In this work, a sandwich vertical tunnel field effect transistor (SDG-VTFET) is presented and studied. Since the dominant carrier tunneling of SDG-VFET occurs in a direction that is in line with the gate field, high ON-state current and steep subthreshold slope are observed. Comparisons between SDG-VFET and double gate tunnel field effect transistor are made to clarify advantages of SDG-VTFET. The simulation results of our work show that SDG-VTFET has stronger gate control, steeper subthreshold slope and higher ON-state current. The device plays a promising candidate for future low power circuit applications.

1. Introduction

With the development of the integrated circuit, power consumption becomes more and more serious. Tunnel field-effect transistor (TFET), which has a different current injection mechanism from MOSFET, is proved to be an attractive candidate for further scaling of the supply voltage V_{DD}. High ON-sate current (I_{ON}), low OFF-state current (I_{OFF}) and minimized subthreshold swing are critical targets for an excellent TFET device. Because of a large tunneling resistance which due to carrier tunneling between energy states of different symmetry, ON-state current of TFET is much lower than that of MOSFET. To enhance the I_{ON}, much improvement has been reported by the use of a lower bandgap material such as SiGe [1,2], or InAs [3], in the tunneling region, a double-gate architecture [4,5], a high-k gate dielectric [4,6], heterojunction technology [7–9], junctionless TFET [10,11], a thin silicon body [12], vertical TFET [9,13,14], etc.

The ON-state current of TFET is depended on the following parameters: tunneling area and tunneling probability. Conventional lateral P–I–N TFETs are not able to provide large enough drain current even with a low direct band gap such as InAs because of small tunneling area. When the voltage applied to the gate electrode is increased, band bending near the reverse-biased P^+ source-Intrinsic region (P–I) tunneling junction is not very sharp. This results in a larger tunneling barrier width, a lower tunneling probability and a weaker gate modulation to the band-to-band tunneling current. Vertical tunnel field effect transistor, the dominant carrier tunneling of which occurs in a direction that is in line with the gate field, shows higher ON current and steeper subthreshold slope than lateral TFET. However, there is a tunnel channel between drain region and channel region in OFF-state. The tunneling channel deteriorates the leakage in OFF-state. A new kind of TFET which has high ON-state current and low OFF-state current is needed.

In this work, we propose and examine a sandwich double-gate vertical tunnel field transistor (SDG-VTFET). Dominant carrier tunneling of SDG-VTFET of SDG-TFET occurs in a direction that is in line with the gate field. It has larger tunneling area

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http://dx.doi.org/10.1016/j.spmi.2016.03.026
0749-6036/

and sharper energy band diagram than lateral counterpart. A 5 nm thickness Oxide between drain region and source region blocks the lateral tunneling channel in OFF-state. Channel region which is lightly doped is replaced by N^+ region, the concentration of which is the same as drain region. An extended length of gate (L_{GD}) is used to increase the lateral tunneling barrier width to further reduce the OFF-state current. The results of our simulation show that the device has great competition.

2. Basic device concept

The cross sectional view of the proposed sandwich double gate vertical TFET (SDG-VTFET) and a double gate TFET (DG-TFET) structures are shown in Fig. 1 (a), (c), respectively. The length of drain and source regions are both 20 nm, the length of gate L_G varies from 20 nm to 60 nm. The thickness of body is 15 nm, high-k gate dielectric HfO_2 T_{OX} is 2 nm, Source region doping concentration N^+ is 1×10^{18} cm^{-3}, drain region doping concentration P^+ is 1.2×10^{20} cm^{-3}. The gate work function Φ_G is 4.1 eV. The parameters mentioned above are applied to the two devices if no special explanation.

The simulations are performed by using Silvaco TCAD [15]. Since the tunneling process is nonlocal, we use a nonlocal band-to-band tunneling (BTBT) model. The nonlocal band-to-band tunneling model takes into account the spatial variation of the energy bands without the consideration that generation/recombination of opposite types are spatially coincident. The Fermi-Dirac statistics and Shockley-Read-Hall (SRH) recombination model are included for calculation of transport characteristics. Since the drain region and source region are both highly doped, the band gap narrowing model (BGN) is included. Lombardi mobility models (cvt) is included for the mobility effect. Gate leakage is neglected in our simulations. Quantum confinement (QC) model given by Hansch [11,15], is included. We have calibrated our simulation models by reproducing the results reported in Refs. [1,16,17].

3. Simulations results and discussions

Fig. 1 (d) shows energy band diagram of SDG-VTFET in ON-state and OFF-state. The operating principle of SDG-VTFET can be figured out from it. When the voltage is applied to the two gate electrodes and varies simultaneously from 0 V to 1 V to turn the device on, energy band near the tunneling junction bends and tunnel barrier width is decreased. Since the tunneling probability of source electron is depended exponentially on the tunnel barrier width, tunneling current of the source electron is improved. In OFF-state ($V_{GS} = 0$ V and $V_{DS} = 1.0$ V), the tunneling probability is negligible because of a large tunnel barrier

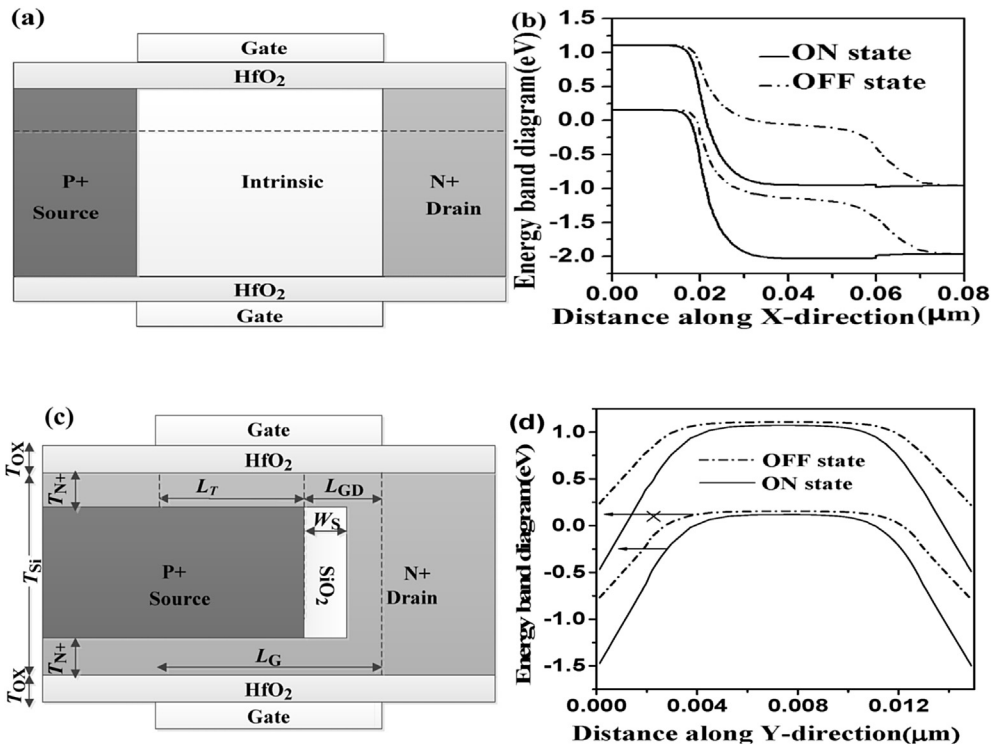

Fig. 1. (a) lateral P^+-I-N^+ double gate TFET (DG-TFET). (b) Energy band diagram of DG-TFET along X-direction in OFF state and ON state(2 nm away from the oxide-silicon interface).(c) sandwich double-gate vertical tunnel field transistor (SDG-VTFET).(d) energy band diagram of SDG-VTFET along Y-direction in OFF state and ON state(30 nm away from the left side). $\Phi_G = 4.1$ eV.