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A novel double gate metal source/drain Schottky MOSFET as an inverter

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ABSTRACT

In this work, we propose and simulate a novel structure of a double gate metal source/drain (MSD) Schottky MOSFET. The novelty of the proposed device is that it realizes a complete CMOS inverter action, which is actually being realized by the combination of two *n* and *p* type MOS transistors in the conventional CMOS technology. Therefore, the use of this device will significantly reduce the transistor count in implementing combinational and sequential circuits. Further, there is a significant reduction in the number of junctions and regions in the proposed device in comparison to the conventional CMOS inverter. Therefore, the proposed device is compact and can consume less power. The proposed device has been named as Sajad-Sunil-Schottky (SSS) device. The mixed mode circuit analysis of the proposed SSS device has shown that a CMOS inverter action with high logic level (V_{OH}) and low logic level (V_{OL}) as ~V_{DD} and ~ground respectively. A two dimensional calibrated simulation study using the experimental data has revealed that the proposed SSS device in *n* and *p* type modes have subthreshold slopes (S) of 130 mV/decade and 85 mV/decade respectively and have reasonable high I_{ON} and I_{ON}/I_{OFF} ratio's. Furthermore, it has been proved that such a device action cannot be realised by folding the conventional doped *n* and *p* MOS transistors.

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1. Introduction

The overwhelming growth of the metal oxide semiconductor field effect transistor (MOSFET) technology in the last four to five decades can be attributed to the scaling of device dimensions. The scaling has significantly increased speed, functionality and packing density and has reduced power dissipation, chip cost etc [1,2]. However, the continuation of scaling below 22 nm technology node is extremely challenging due to short channel effects (SCE), gate tunneling, leakage, channel transport limitations, and most importantly the significant increase in source/drain series resistance [2–4]. The International Technology Roadmap for Semiconductors (ITRS) [7] has predicted that there is no known potential solution for the parasitic S/D resistance challenge beyond 2008 [4,17–24], to keep Moore's law valid for some more years. The use of raised source and drain has alleviated the series resistance problems to some extent; however, it has complicated the fabrication process and has increased the gate to source/drain capacitance [4]. The use of metal source/drain (S/D) or metal silicide S/D architectures provide elegant solutions to series resistance problem, as low contact resistivity and low sheet resistance are obtained

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[4–6,8–16]. Since scaling the dimensions of MOS devices to enhance performance is restricted by SCEs and other issues, therefore, it is wise to go for the architectural changes in devices to enhance the performance and functionality.

In this paper, we propose a new structure of a double gate metal silicide S/D Schottky MOSFET with improved performance. The device is novel in a way that in spite of being a single transistor, it is capable of realizing a complete inverter action, which normally needs two separate transistors. Further, it can be used as an *n* or *p* type transistor also and is the first metal S/D based MOSFET to work efficiently as *n*MOS, *p*MOS and an inverter, to the best of our knowledge. Its use as an inverter will result in a significant increase in packing density, functionality, reduced power and will significantly reduce the requirement of transistor count in implementing other gates. The proposed device has been named as Sajad-Sunil-Schottky (SSS) device. The proposed SSS device has reduced number of junctions, regions, contacts, uses a single substrate in comparison to the conventional CMOS inverter. It integrates functionality of electron and hole channels on a single silicon substrate; hence an inverter action is implemented at the device level of abstraction. Further, apart from providing an elegant solution to the series resistance problem in a nanoscaled device, the use of metal S/D will significantly reduce the thermal budget in the proposed device fabrication, as no *n* and *p* type doping is involved, as in a conventional CMOS technology. Further, since our proposed SSS device employ metal S/D regions, therefore random statistical variations in positioning of S/D contacts to the channel region due to doped diffusion effects are eliminated in comparison to the conventional doped CMOS devices [4,24]. Furthermore, since the proposed device is multifunctional and has improved SCE suppression capability, therefore, it will significantly extend Moore's law validity further.

2. Schematics and the simulation setup

The schematic of the proposed SSS device is shown in Fig. 1. It is a double gate device with top gate (TG) optimized work function of 4.45 eV and bottom gate (BG) optimized work function of 4.95 eV. The work functions of gates are chosen so that the proposed SSS device has optimum I_{ON}/I_{OFF} ratios in both *n* and *p* modes of operation. The TG controls the *n*-mode action and the BG controls the *p*-mode action. Erbium silicide (ErSi1.7) is acting as source and drain in the *n*-mode operation and the platinum silicide (PtSi) is acting as source and drain in the *p*-mode operation, as shown in Fig. 1. The use of silicides such as platinum silicide (PtSi) ($\Phi_{b,h}$ ~ 0.15–0.27eV) and erbium silicide (ErSix) or ytterbium silicide (YbSix) ($\Phi_{b,e}$~0.27–0.36 eV) results in lowest known Schottky barrier heights with silicon respectively [4]. The proposed SSS device uses a common substrate for both *n* and *p* channels as compared to two different substrates for a.conventional CMOS inverter, as shown in Fig. 1(b). The use of a common substrate and metal silicide S/D results in a significant reduction in number of junctions in comparison to a conventional CMOS inverter. Further, since drains in both modes are metal silicides and are in close contact, so there is no need of an extra path to make a contact of two separate drains, as is needed in a conventional CMOS inverter. The two sources in the proposed SSS device are isolated by silicon dioxide (SiO_2). Further, on comparing the proposed SSS device with the conventional CMOS inverter, as shown in Fig. 1(b), it is clear that a significant reduction in junctions, wells, oxide regions is achieved in the proposed device. These reductions will result in a compact SSS device, with reduced power

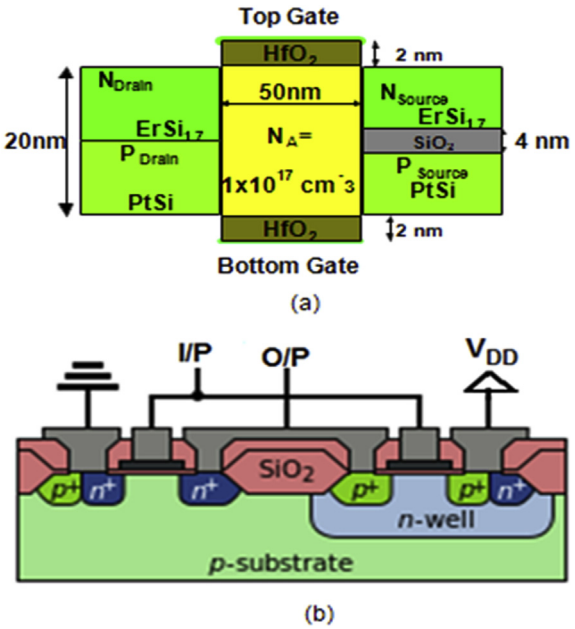

Fig. 1. (a) Schematic diagram of the proposed Sajad-Sunil-Schottky (SSS) device (b) conventional CMOS inverter.

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