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Investigation of dielectric pocket induced variations in tunnel field effect transistor

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ABSTRACT

The performance of conventional Tunnel FETs struggling from ambipolar issues, insufficient on-current, lower transconductance value, higher delay and lower cut off frequency has been improved by introducing several material and device engineering concepts in past few years. Keeping this in view, another interesting and reliable option i.e. Dielectric Pocket TFET (featuring a dielectric pocket placement near tunneling junction) has been comprehensively and qualitatively demonstrated using ATLAS device simulator. The architecture has been explored in terms of various device electrostatic parameters such as potential, energy band profile, electron and hole concentration, electric field variation and band to band generation rate (G_{BTB}) near the tunneling junction where the Dielectric Pocket (DP) has been introduced. Subsequently, a detailed investigation by changing the position and dielectric constant of pocket at respective junctions has been made where DP induced variations in drain current, transconductance and parasitic capacitance have been examined. The work highlights major improvements over conventional TFET in terms of lower subthreshold swing and threshold voltage, higher drain current and transconductance, improved on-to-off current ratio, suppressed ambipolar conduction and improved dynamic power dissipation issues for low voltage analog and digital applications.

1. Introduction

In last few years, Tunnel FETs (TFETs) have been looked upon as one of the possible device design for future energy efficient and cost effective applications. Being listed among various possible alternatives, TFETs have been considered as an alternative choice because of its Band to Band Tunnelling (BTBT) conduction phenomenon which helps in lowering the Subthreshold Swing (SS) and various Short Channel Effects (SCEs) [1]. Unlike MOSFETs (whkich are limited to SS value of 60 mV/decade and static power leakage in case of highly scaled low power devices), TFETs offer a significant power reduction with sufficiently lower off-current (I_{off}) [1]. Conventional p-i-n TFET suffers from severe drawbacks like low on-current (I_{on}), higher ambipolar current (I_{amb}), low transconductance (g_m) and higher delay (τ_{delay}) which limits its utility for digital applications. In order to

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circumvent such major issues, alternative TFET architectures have been reported namely pocket source TFET with heavily doped pocket region in between source and channel [2], Hetero-Dielectric TFET [3], Dual Material Gate Hetero-Dielectric TFET [4], low band gap materials based [5], Hetero-Junction TFET [6] etc. Likewise scaling gate dielectric thickness is another option to improve the device control but it results in enhancing gate leakage current thereby affecting the standby power dissipation. Thus, High-k dielectric seems to be a better option but may lead to problems like interface trap generation and hence affecting its reliability performance. Subsequently reducing the channel thickness would result in improving I_{on} but simultaneously, it would also increase the I_{amb} and quantum confinement related effects.

Such critical impediments have been suppressed in one of the recently proposed TFET configuration [7,8] with the introduction of a Dielectric Pocket (DP) at source/channel junction of conventional p-i-n TFET. The architecture is expected to be suitable for future low power applications and can be fabricated using recently proposed techniques [9] for TFET. Interestingly, FET based studies incorporating dielectric pocket have also been reported [10,11] where the role of dielectric pocket has been shown to improve the SCEs, current driving capability and junction capacitances because of higher effective channel length. The proposed architecture i.e. DP TFET (having dielectric pocket at source/channel junction) [8] is capable of delivering comparatively higher I_{on}, suppressed SS, lower threshold voltage value (V_{th}), higher g_m, high I_{on}/I_{off} with a significant reduction in parasitic capacitance values. Our previous analysis [8] provided a detailed investigation to improve the device efficiency by tuning the pocket dimensions (t_{pocket} and h_{pocket} in Fig. 1(b)) and dielectric constant (for both pocket and gate dielectric at Si/SiO_2 interface). However, the analysis regarding pocket induced variations in device electrostatics is still an important subject to explore. Keeping this in view, a detailed simulation study to investigate for such Figures of Merit (FOM) has been carried out in present work. Simultaneously, the architecture i.e. DP TFET has been studied and compared with conventional p^+ p^- n^+ TFET (***Case-1***) by changing the pocket positions as: ***Case-2*****:** DP TFET with Pocket at source/channel junction inside source region, ***Case-3*****:** DP TFET with Pocket at source/channel junction inside channel region, ***Case-4*****:** DP TFET with Pocket at drain/channel junction inside channel region and ***Case-5*****:** DP TFET with Two Pockets at source/channel and drain/channel junction inside channel region. The work has been extended to demonstrate the benefit of changing the dielectric constant of pocket near drain edge.

2. Simulation details and model calibration

The schematic diagram of a conventional TFET and DP TFET has been represented in Fig. 1(a) and (b) respectively having channel thickness (t_{si}) of 10 nm, gate oxide thickness (t_{ox}) of 3 nm and channel length (L_{ch}) of 50 nm if not stated otherwise. The source and the drain regions have been symmetrically and abruptly doped having doping concentration of $1 \times 10^{20}/cm^3$. The channel region is kept to be lightly p-type doped with a concentration of $1 \times 10^{15}/cm^3$. In Fig. 1(b), the pocket thickness,

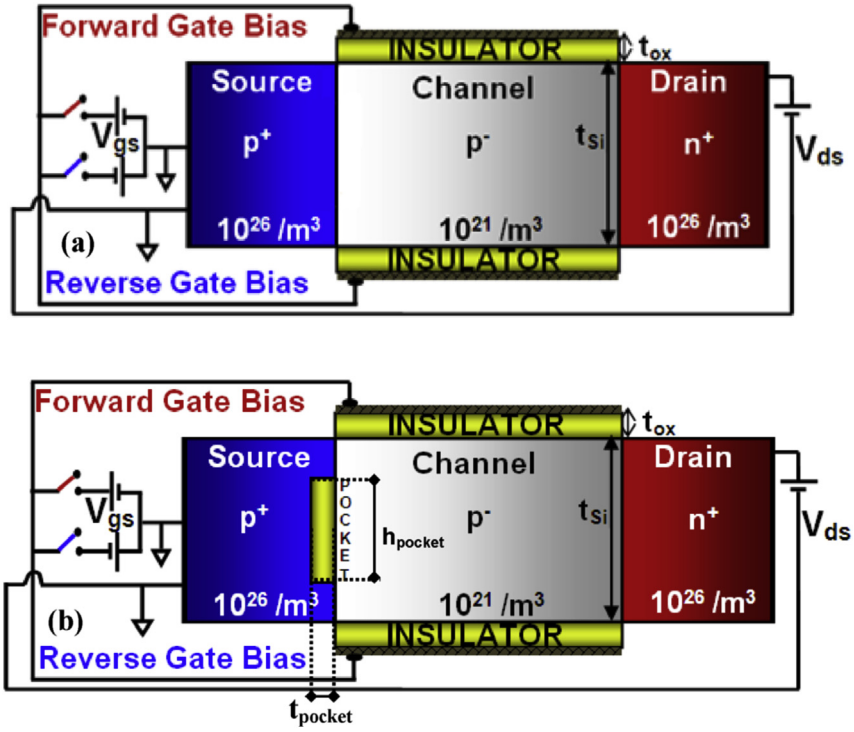

Fig. 1. (a) Conventional TFET architecture, (b) Dielectric Pocket (DP) TFET architecture.