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# Two-dimensional model of a heterojunction silicon-on-insulator tunnel field effect transistor

Sweta Chander*, S. Baishya

*Department of ECE, NIT Silchar, Silchar 788010, India*

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ABSTRACT

In nanoscale regime, Tunnel field effect transistor (TFET) is the most promising candidate as it provides smaller subthreshold swing (SS) and higher $I_{on}/I_{off}$ ratio than conventional MOSFET. We propose a two-dimensional analytical model for a heterojunction silicon-on-insulator (SOI) TFET using an infinite series solution technique. Analytical expressions for the electrostatic potential, electric field, and energy band are developed by solving 2D Poisson's equation under appropriate boundary conditions. The impact of gate length scaling on the surface potential profile is also analyzed and studied. The electric field is used to calculate the drain current. The derived analytical expressions are validated with Synopsys TCAD results.



## 1. Introduction

One of the major concerns due to the miniaturization of the MOS transistors is the increased power consumption [1]. Reducing the supply voltage requires that the threshold voltage be scaled down proportionately in order to achieve the same performance of the device. This decreased threshold voltage, in turn, increases the subthreshold leakage which become a dominant component of power consumption. This problem, however, can neither be solved by novel MOS structures nor by material engineering. Such inherent limitation of MOS transistors in nanoscale regime can, to a large extent, be overcome by emerging devices like Tunnel FET [1], FinFET [2], Silicon Nanowire FET (SiNWTFET) [3], CNTFET [4] where techniques like gate engineering, junction engineering, channel engineering etc. are applied. Among them, the Tunnel FET exhibits unidirectional conduction, steep slope, and delayed saturation characteristics due to the asymmetric P–I–N structure and can easily be fabricated. Furthermore, they consume low power which is more appropriate for energy-constrained applications [5]. TFETs with homo-junctions do not show satisfactory results in terms of on current, steep SS etc. because of the limitations in physical properties such as bandgap of the single material [6–8]. In this regard, heterojunction TFETs using group IV and III–V semiconductors have drawn lot of attraction. Group III–V semiconductors can provide high performance n-channel TFETs, but the performance of p-channel devices is limited by the low conduction-band density-of states [9–11]. Moreover, the in-compatibility with Si processing and the poor high-k interface are still the main limitations for III–V TFETs. Possibly to avoid the incompatibility issue, the research is more focused on hetero-junction TFETs based on group IV materials, such as Ge/Si [12,13], Ge/Strained-Si [14], strained Si [15,16], strained Ge [17], strained SiGe [18–21], and GeSn [22]. In our previous work [11], we reported performance improvement and gate threshold voltage modeling of such heterojunction devices.

* Corresponding author.
*E-mail address:* sweta.chander@gmail.com (S. Chander).

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From the fabrication point of view as well, germanium can easily be integrated into the conventional CMOS processes by adapting the well-developed silicon process technology. Compared to fabrication and numerical simulation [12,14,23,24], the pace of model development for TFET is very slow. For circuit design applications, there is a lot of demand for accurate physics-based analytical models. As the device dimensions are scaled to nanometer regime, the 1D approaches [25,26] are not expected to give acceptable results, while the most of the 2D approaches for double gate structures use a simplified delta approximation approach [27,28]. To study the band-to-band tunneling (BTBT) mechanisms of the TFET, more accurate 2D models for TFET are needed for circuit design applications. More rigorous 2D models [29,30] works are primarily applicable for homo-junction devices only.

In this paper, we report 2D models for heterojunction SOI-TFET. We solved the 2D Poisson's equation, with suitable boundary conditions, and derived the analytical expressions for electrostatic potential, electric field, and energy bands. The developed expressions are used to calculate the drain current with the help of numerical integration. The model calculations are validated with TCAD simulation results.

## 2. Device structure and simulation methodology

Fig. 1(a) shows a schematic diagram of a 30 nm n-type heterojunction SOI-TFET with oxide overlap on Ge source region. Doping concentrations of source, channel, and drain are $10^{19}$, $10^{16}$ and $10^{19}$ $cm^{-3}$, respectively. In our device, we used the optimized oxide thickness ($t_{ox}$) of 4 nm and body thickness ($t_{si}$) of 20 nm. To reduce the interface problem between $HfO_2$ and silicon, stacked $HfO_2/SiO_2$ is used with equivalent oxide thickness (EOT) of 1.4 nm as the gate dielectric material. Aluminum with work function of 4.1 eV is used as the gate material. When the thickness of the gate oxide ($SiO_2$) is less than 1.3 nm then the device performance decreases due to enhanced leakage [31]. The solution to the above problem is achieved by using high-κ material since it suppress the gate leakage current and at the same time it maintains the same oxide capacitance. $HfO_2$ is a very promising high-κ material and has several advantages in the formation of gate dielectric layer. However, the interface property of $HfO_2$ is not very satisfactory with silicon. Therefore, $SiO_2$ is necessary to use at the interface [32,33]. Moreover, the $SiO_2$ can not only help to reduce the thermodynamic instability between high-κ materials and Si, but also accommodates the difference in lattice constants between Si and another materials [34]. Accordingly, we have used the gate dielectric as a stacked $HfO_2/SiO_2$, with Equivalent Oxide Thickness (EOT) of 1.4 nm. Aluminum with work function of 4.1 eV is used as the gate material. Stacked Al/High-k/$SiO_2$ is also used to reduce the stand-by power leakage [35]. High-k spacer ($HfO_2$) is used for performance improvement of the n-channel heterojunction TFETs. In addition to heterojunction, such spacer helps to produce an enhanced ON current without degrading OFF state current and subthreshold swing [36].

In non-local BTBT model, the conduction and valence bands are multi-dimensionally traced to get the path for tunneling. As shown in Fig. 1(b), the average electric field along the traced tunnel path is defined as the nonlocal electric field ($E_{nonl}$), and is given by Ref. [37]:

$$E_{nonl} = \frac{E_G}{L} \tag{1}$$

where $E_G$ is the band gap and $L$ is the tunneling length which is the traced distance from the valence band edge ($E_V$) to the conduction band edge ($E_C$) at the same level along the tunneling path. We have used non-local BTBT model without bandgap narrowing effect.

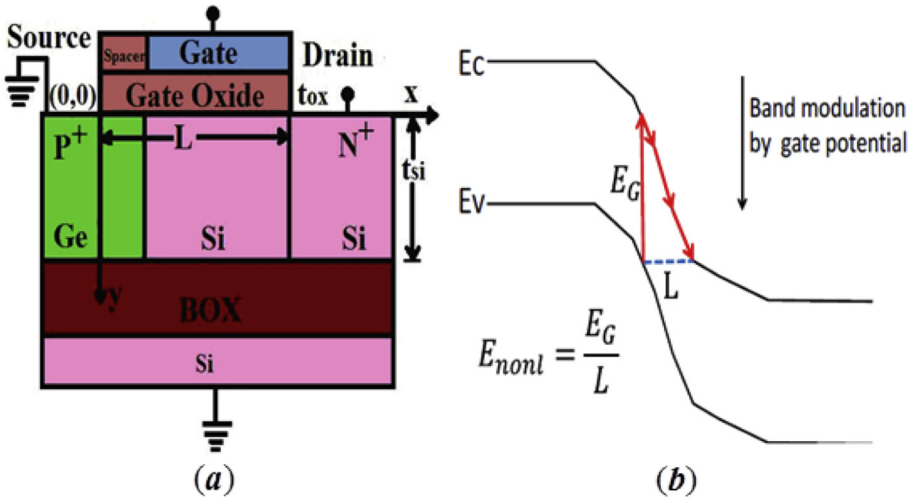


**Fig. 1.** (a).Cross sectional view of the proposed device and (b) Non-local electric field using band diagram [37].