Superlattices and Microstructures 80 (2015) 20–31

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Analytical model of gate leakage current through bilayer oxide stack in advanced MOSFET

Rathin Basak [a,*], Biswajit Maiti [b], Abhijit Mallik [c]

[a] Department of Physics, Kalyani Govt. Engineering College, Kalyani, Nadia, West Bengal, India
[b] Department of Physics, Darjeeling Govt. College, Darjeeling, West Bengal, India
[c] Department of Electronic Science, University of Calcutta, West Bengal, India

ARTICLE INFO

Article history:
Received 12 December 2014
Accepted 17 December 2014
Available online 30 December 2014

Keywords:
Density of states
Fowler–Nordheim tunneling
MOSFET
Quantum tunneling
Quantum well
Tunneling probability
WKB approximation

ABSTRACT

A compact model for gate tunneling current in advanced nano-scale MOSFET has been developed on the basis of both direct and Fowler–Nordheim tunneling through dual layer Silicon oxide–Hafnium oxide stack used as gate dielectric. Calculation includes the effect of different subbands of the semiconductor conduction band those arise due to quantum confinement of charge carriers in the oxide–substrate interface. Effect of charge trapping in the bulk of the oxides and at the localized energy levels at different interfaces of the oxides has also been taken into consideration. Tunneling probability as a function of gate bias has been determined considering Wentzel–Kramers–Brillouin (WKB) approximation to account for varying potential profile. Probability amplitude of an electron for tunneling has been calculated by solving Schrodinger equations at different regions in the effective mass approximation model of class I crystal interface. Tunneling current as a function of effective oxide thickness and gate bias estimated in this model shows substantial reduction in gate leakage current if HfO_2 as high-k dielectric is used along with 1 nm thick SiO_2 with almost negligible change in threshold voltage.

1. Introduction

PRESENT generation MOSFET technology is using 45 nm-node or below that. As a result of this aggressive decrease in dimension, gate leakage current is increased to a large extent and also the reli-

* Corresponding author.
E-mail address: basak_rathin@yahoo.co.in (R. Basak).

http://dx.doi.org/10.1016/j.spmi.2014.12.018
0749-6036/

ability and control over the device is being affected. When SiO_2 thickness is reduced below 2 nm, in traditional MOS device, the leakage current density may go beyond 10A/cm^2 [1]. Beside the adverse effect of high direct tunneling current, there is the problem of Boron diffusion into and through oxide layers from poly-Si gate electrode in p-channel devices even at low electric field [2]. This severely degrades the device performance over time. So people think of using different high-k dielectric materials like La_2O_3, ZrO_2, HfO_2 etc. instead of SiO_2 alone. Among the rare earth oxides HfO_2 is the most promising high-k dielectric material because of its good thermal stability with Si. Introduction of the rare earth oxides help in reducing gate-leakage current to some extent but in the turn device reliability is affected from defect states inherent to these materials. These defect states act as trap centers which are mainly accumulated near the interfacial layers, as a result the mobility of electrons along the MOS channel is affected [3]. Also mechanical strain generated due to lattice mismatch between Si substrate and rare earth oxide over layer causes the trap centers to be distributed along the interface. To circumvent this problem stacked films of oxides/nitrides as high-k dielectrics on thin SiO_2 layer have gain much attention in recent years [4–8]. It is very important to maintain the quality of the interfacial layers in high-k gate dielectric stacks those often act as critical factors in affecting the transistor performance and reliability [9].

Ultra thin gate oxide and high substrate doping concentration in these MOSFETs create very high electric field at the oxide–semiconductor interface that causes severe band bending at the interface. The width of electron accumulation/depletion layer near the interface is too narrow to cause energy quantization and the resulting 2D electron gas tunnels through thin oxide layers constituting major part of gate tunneling current. The quantum tunneling in MOS devices has often been analyzed through direct tunneling [10–12], Fowler–Nordheim tunneling [13,14], trap-assisted tunneling [15–17]. In most of the cases, semi-empirical model involving solution of Schrodinger–Poisson equation has been used [18,19] to determine the current–voltage characteristics and the tunneling characteristics in MOS devices.

Wu et al. [20] have introduced a modified semi-empirical relation based on WKB approximation and quantum mechanical simulation based on three-subband model to study the gate voltage and surface potential dependence of gate leakage current density for different high-k dielectrics. They have showed that direct tunneling is the dominant mechanism at low voltages. However, in their calculation of electron energy level, well known triangular potential well approximation has been used. Later, Mondal et al. [21] has modified the energy expression by considering electric field penetration inside the bulk of the substrate. The result showed a 25% decrease in the ground state energy of electron in the potential well at the interface. In their article they have truly taken the approach of calculating wave function of inversion layer electrons and found non-zero value at the interface. This is indicative of tunneling of electrons into the oxide layer. This approach is quite different from most of the others found in literatures [22] but we find it to be physically more correct in devising a fully analytical model for gate tunneling current.

Over the last decade substantial amount of works have been dedicated to finding an effective analytical, rather semi-empirical model those represent physical basis for the performance of multi-oxide nano-MOS device. But a simple fully analytical model that encompasses all the controlling parameters of these devices is still to be developed. In this article we have tried to analyze the effectiveness of SiO_2-HfO_2 stack as a viable alternative and have tried to determine the effective electron density at the semiconductor oxide interface more accurately by taking into account the variation of inversion layer thickness with gate bias and in turn, its effect on the subband energy levels. The article is organized in the following way: In section-II, Schrodinger equation is solved rigorously at different regions considering exact potential profile from gate to substrate. The effect of gate biasing, band offset, substrate doping concentration, quantum confinement effects at the inversion layer and trap states distribution at the interfaces and in oxides have been taken into account to determine the exact potential profile. Then an analytical model for gate tunneling current is derived considering corrected electron flux density appearing at the oxide interface. Regime of different tunneling mechanisms depending on gate bias has been investigated. In this way a fully analytical model with no fitting parameter has been formulated in section-II. In section-III, gate-tunneling current as a function of gate bias and effective oxide thickness have been demonstrated. Finally we make our conclusion in section-IV.