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Nanoscale T-shaped Double Gate DG MOSFET: Numerical Investigation for Analog/RF and Digital Performance

Vandana Kumari [a, b], Aravindan Ilango [c], Manoj Saxena [d], Mridula Gupta [a, *]

[a] Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi, South Campus, New Delhi, India
[b] Department of Electronics, Maharaja Agrasen College, University of Delhi, India
[c] Cisco Systems (India) Private Limited, SEZ Unit, Cessna Business Park, Bengaluru, Karnataka, India, 560103
[d] Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, India

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ABSTRACT

The present work demonstrates the investigation of T-shaped Double Gate MOSFET for analog and digital performance. The 2D analytical modeling scheme is presented using Evanescent Mode Analysis (EMA). The applicability of the proposed model has been verified using ATLAS 3D device simulation. The device exploits peaks in the electric field inside the channel (due to T-shaped gate) for better carrier transport efficiency and subsequently higher drain current and trans-conductance. The impact of dielectric constant of the void layer (due to T-shaped gate) on the electrostatic of the device has been investigated using basic electrical parameters such as: sub-threshold slope, Drain Induced Barrier Lowering DIBL, device gain and I_{on}/I_{off} ratio. The comparative study between T-shaped DG with the conventional DG MOSFET is also presented.

1. Introduction

For the last four decades, Planar MOSFETs have been of paramount importance for the silicon industry. MOSFET scaling has been governed by Moore's Law, but the scaling trend has shown some deviation as the device dimensions reached sub 90 nm technology node. The continuous scaling of device dimensions has resulted in alleviating Short Channel Effects (SCEs) such as Threshold voltage roll-off, poor subthreshold slope and hot-electron effects. In addition to this, shorter the gate length, higher will be the gate resistance [1]. As per ITRS, there has been a paradigm shift in tackling these problems and emphasis is on studying ERD (Emerging Research Devices) [2]. Multiple Gate FETs (MuGFETs) falls in the category of ERD and are also able to counter the SCEs by means of additional gates which provides better gate control over the channel. There is a multitude of MuGFET architectures found in literature such as Double Gate [3], Triple Gate [4], Quadruple-Gate [5], FinFET [6], Pi-Gate [7], Omega-Gate [8], Rectangular GAA(Gate-All Around) [9], Spherical GAA [10], etc. Inspite of these innovative devices, in 2004, Lee et al. proposed a new gate architecture i.e. T-shaped Gate on the bulk MOSFET [11]. The proposed architecture successfully lowered the associated gate capacitance as well as the gate resistance. Moreover, Furukawa et al. in 2007, have successfully fabricated the T-shaped gate on silicon wafer [12]. In 2010, Lee et al. utilize the benefits of T-shaped gate on DG geometry for 4-bit SONOS type nonvolatile memory [13] wherein Gate Induced drain Leakage (I_{GIDL}) current read method was used to

* Corresponding author.
E-mail addresses: vandanakumari511@gmail.com (V. Kumari), aravindanilango93@gmail.com (A. Ilango), saxena_manoj77@yahoo.co.in (M. Saxena), mridula@south.du.ac.in (M. Gupta).

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make the device more sensitive towards locally stored charges within the gate-dielectric stack. They also discussed the fabrication flow of the proposed device architecture. Therefore in the present work, we analyse the influence of T-shaped gate on the electrical parameters of Double Gate architecture. The gate leakage current and the impact of interface charges are neglected in the present work. The main focus of our study is to understand the impact of T-shaped geometry on the multigate architecture. Thus on the basis of our previously reported work [14], we have developed the analytical model for T-shaped Double Gate MOSFET in which Evanescent Mode Analysis (EMA) has been taken into consideration [15]. The various parameters relevant for understanding the behavior of the device for digital (device gain, noise margin, switching current and propagation delay) as well as for analog (trans-conductance, device efficiency and early voltage) applications are studied in this work through exhaustive device simulation.

The complete work presented in this paper is summarized as: Section II describes the analytical modeling approach considered in this work. In Section III, results based on the developed analytical model are compared with the simulated results obtained from the ATLAS 3D device simulator [16]. Section IV describes the comparison between T-shaped DG with the conventional DG MOSFET. The dependence of analog as well as the digital performance metric on the dielectric constant of the void layer (due to T-shaped Gate) (ε_{void}) has also been discussed in this section.

2. Analytical modeling

The schematic cross-sectional view of the T-shaped DG MOSFET is shown in Fig. 1a and the flow chat to describe the modeling scheme is shown in Fig. 1b.

Two dimensional modeling approach based on EMA technique has been employed in this paper. The 2D Poisson's equation in the channel can be written as [17]:

$$\frac{d^2\phi_{ij}(x,y)}{dx^2}+\frac{d^2\phi_{ij}(x,y)}{dy^2}=\frac{qN_{ij}}{\varepsilon_{ij}} \tag{1}$$

Where i denotes the ith region from source to drain region, N_{ij} is the doping concentration, ε_{ij} is the permittivity of the respective regions.

The potential in the channel $\phi_{ij}(x,y)$ can be represented as:

$$\phi_{ij}(x,y)=\phi_{Lij}(y)+\phi_{sij}(x,y) \tag{2}$$

where $\phi_{Lij}(y)$ is the 1D potential and $\phi_{sij}(x,y)$ is the 2D potential which satisfies the Poisson's and Laplaces's equation respectively as given below:

$$\frac{d^2\phi_{Lij}(y)}{dy^2}=\frac{qN_{ij}}{\varepsilon_{ij}} \tag{3}$$

$$\frac{d^2\phi_{sij}(x,y)}{dx^2}+\frac{d^2\phi_{sij}(x,y)}{dy^2}=0 \tag{4}$$

The solution of the 1D Potential in all three regions (transverse) is given by:

$$\phi_{Lij}(y)=\frac{qN_{ij}}{2\varepsilon_{ij}}\left(\sum_{j=1}^{i}t_{ij}-y\right)^2+a_{ij}\left(\sum_{j=1}^{i}t_{ij}-y\right)+a_{ij}\quad 1\le i\le 3 \tag{5}$$

where i denotes the corresponding region in the channel i.e. source to drain and j represent the direction from gate to gate, N_{ij} represents the doping concentration, ε_{ij} represents the permittivity in different regions. The flow chart for calculating the channel potential along with the drain current for T-shaped DG MOSFET is shown in Fig. 1b. The thickness of the various regions is shown in Table 1.

The various boundary conditions necessary to solve the 1D Poisson's equation are:

At the top gate and oxide interface,

$$\phi_{Li1}(0)=V_{gs_1}-V_{fb_1}=\phi_{gs_1} \tag{6a}$$

where V_{gs1} is the gate-source voltage and V_{fb1} is the flat-band voltage for the gate1.

At the bottom gate and oxide interface,

$$\phi_{Li3}(t_{i1}+t_{i2}+t_{i3})=V_{gs_1}-V_{fb_2}=\phi_{gs_2} \tag{6b}$$

where V_{gs2} is the gate-source voltage and V_{fb2} is the flat-band voltage for the gate2.