Superlattices and Microstructures 89 (2016) 120–135

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Design and simulation of oxide and doping engineered lateral bipolar junction transistors for high power applications

Sajad A. Loan [a, *], Faisal Bashir [a], M. Saqib Akhoon [b], Abdulrahman M. Alamoud [c]

[a] Department of Electronics and Comm. Engineering, Jamia Millia Islamia, New Delhi, India
[b] Department of Electronics and Comm. Engineering, IUST, Srinagar, Kashmir, India
[c] Department of Electrical Engineering, King Saud University, Saudi Arabia

ARTICLE INFO

Article history:
Received 20 September 2015
Received in revised form 24 October 2015
Accepted 27 October 2015
Available online 2 November 2015

Keywords:
Silicon-on-insulator
Lateral bipolar junction transistor
Breakdown voltage (BV)
Buried oxide
On-resistance (R_{ON})
Thermal analysis

ABSTRACT

In this paper, we propose new structures of lateral bipolar junction transistor (LBJT) on silicon on insulator (SOI) with improved performance. The proposed devices are lateral bipolar transistors with multi doping zone collector drift region and a thick buried oxide under the collector region. Calibrated simulation studies have revealed that the proposed devices have higher breakdown voltage than the conventional device, that too at higher drift doping concentration. This has resulted in improved tradeoff between the on-resistance and the breakdown voltage of the proposed devices. It has been observed that the proposed device with two collector drift doping zones and a buried oxide thick step results in ~190% increase in the breakdown voltage than the conventional device. The further increase in the number of collector drift doping zones from two to three has increased the breakdown voltage by 260% than the conventional one. On comparing the proposed devices with the buried oxide double step devices, it has been found that an increase of ~15–19% in the breakdown voltage is observed in the proposed devices even at higher drift doping concentrations. The use of higher drift doping concentration reduces the on-resistance of the proposed device and thus improves the tradeoff between the breakdown voltage and the on-resistance of the proposed device in comparison to buried oxide double step devices. Further, the use of step doping in the collector drift region has resulted in the reduction of kink effect in the proposed device. Using the mixed mode simulations, the proposed devices have been tested at the circuit level, by designing and simulating inverting amplifiers employing the proposed devices. Both DC and AC analyses of the inverting amplifiers have shown that the proposed devices work well at the circuit level. It has been observed that there is a slight increase in ON delay in the proposed device; however, the OFF delay is more or less same as that of the conventional device.

1. Introduction

Bipolar-CMOS (BiCMOS) technology integrates the high speed bipolar technology and low power MOS technology on the same substrate. As a result, a BiCMOS gate has higher drive capability than a CMOS gate, while maintaining low power consumption. BiCMOS is able to realize VLSI circuits with speed-power-density performance previously unattainable with

* Corresponding author.
E-mail addresses: sloan@jmi.ac.in, sajadiitk@gmail.com (S.A. Loan).

http://dx.doi.org/10.1016/j.spmi.2015.10.042
0749-6036/

either CMOS or bipolar technology individually. For BiCMOS technology, CMOS remains the backbone for building digital part of a system and bipolar technology is used for the realization of radio frequency (RF) and analog functions. However, the main concern of the state-of-the-art BiCMOS technology is the cost and complexity of the technology, due to incompatibility of the bipolar and MOS technologies. The implementation cost of the state-of-the-art 0.1 μm SiGe BiCMOS technology could easily be more than five times when compared to 0.35 μm SiGe BiCMOS technology. The cost will be huge for nanometer range BiCMOS technologies [1,2]. The BiCMOS on bulk substrate is comparatively cheap; however, poor isolation, cross talk, higher capacitance, need of deep trenches are some important issues with this technology.

The drivers of BiCMOS technology are mixed signal systems, such as, a system on chip (SoC). In a SoC, analog and digital domains are realized on a single substrate. SOI has become a substrate of choice for BiCMOS technology, as it offers advantages in terms of reduction of parasitic capacitance, reduction in crosstalk, high speed, perfect DC and AC isolation etc. [3,4]. High voltage devices fabricated on a SOI substrate are of great interest for application in automobiles, aircrafts, motor control and lightening due to their superior radiation hardness abilities and perfect dielectric isolation with low leakage current [3–5]. However, higher costs and longer fabrication cycle time are some major issues with the SOI-BiCMOS technology. This can be attributed to the difficulty in integrating vertical bipolar junction transistor with SOI-CMOS. The vertical bipolar device requires the SOI layer to be thicker (>1 μm) under the collector region. This results in an additional cost of the SOI wafers and compatibility problems with the thin film SOI [5,6]. The SOI substrate is a real cost adder, however, no sub-collector, no epitaxial layer and no deep trenches as the cost subtractors.

The various issues with the BiCMOS technology are addressed by replacing vertical bipolar junction transistor (BJT) by a lateral bipolar junction transistor (LBJT) on SOI. The LBJT on SOI possess many advantages, such as low power consumption, high breakdown voltage and low parasitic capacitances [7–10]. Further, lateral bipolar transistors are ideally suited to thin film SOI, resulting in simpler device integration and have a potential to share fabrication steps with the MOS technology without performance degradation [9,10]. Unfortunately, lateral bipolar junction transistors have poor current gain (β) and cutoff frequency (f_T) due to limitations related to the base width and the base series resistance [9,10]. The drawback of poor f_T in the lateral BJT demands that the on-resistance of the device must be minimized. However, the on-resistance and the breakdown voltage are inversely related to each other, as per the reduced surface (RESURF) effect [9–14]. Decreasing the on-resistance of a device demands that the drift doping concentration must be increased, which results in a decrease in breakdown voltage. Therefore, there is a tradeoff between the on resistance and the breakdown voltage of LBJT on SOI device, which needs to be improved [11–13].

Several ideas have been used to enhance the breakdown voltage of lateral bipolar devices. They include reduced surface field (RESURF) principle [13], fully depleted collector drift region [14], graded drift region [15,16], semi insulating polysilicon (SIPOS) passivation layers [17–19], buried oxide step structures [9] and extended box in lateral Schottky transistor [8,20]. The concept of multi doping zones and multistep oxide has also been used in to increase the breakdown voltage of a lateral bipolar transistor [9,22,25]. However, it is always a challenge to device designers to get high breakdown voltage in a thin film LBJT on SOI. To obtain large breakdown voltage in LBJT on SOI, the lateral surface electric field distribution along the silicon surface must be uniform. However, it is quite difficult to obtain perfect uniformity in the surface electric field distribution. The experimental and theoretical results have shown that a linearly varying drift doping or linearly varying oxide or combination of both in a thin film LBJT on SOI device results in a perfectly uniform surface electric field distribution and hence maximum breakdown voltage [9,21–25]. However, realizing a device with linearly varying drift doping or linearly varying oxide is extremely difficult, as it needs a large number of precise masking and photolithography steps, exact implantation and drive-in schedules [9,22–24].

The focus of this work is to improve the breakdown voltage of lateral bipolar junction transistors on SOI and to improve the tradeoff between the breakdown voltage and the on resistance. We propose and simulate various structures of LBJT with multizone doped drift region on buried oxide thick step (BOTS) [9,22,25]. A two dimensional (2D) calibrated simulation study of the proposed and the conventional devices have been performed by Atlas simulators. The simulation study is experimentally validated by replacing the default model parameters of Atlas device simulator by the experimental values reported in Ref. [27]. The calibration is done in such a away so that the Gummel plot, current gain and cutoff frequency of the proposed devices match with the experimental results reported in Ref. [27]. Through the calibrated simulation study, the effect of the combination of multizone doping and buried oxide thick step on the breakdown voltage of the device is studied. The simulation study has shown an increased uniformity in the lateral surface electric field in the drift region, reduction of base-collector junction electric field by using lower doping concentration near the junction and enhancement of breakdown voltage in the proposed device.

In this work, three types of lateral bipolar junction transistors on SOI are designed and simulated. They include a device with two zone doped drift region without using BOTS. This is being called as the conventional device. A second type of device uses two drift doping zones and a BOTS. This is being called as two zone proposed (2 ZP) device. The third type of device uses three drift doping zones and a BOTS. This is being called as three zone proposed (3 ZP) device. The simulation results have shown that the 2 ZP device has a breakdown voltage of more than 190% higher than the conventional device. The 3 ZP device possesses breakdown voltage ~260% higher than the conventional one. It has been observed that increasing the number of drift doping zones further increases breakdown voltage marginally but increases the complexity of the device significantly. Therefore, there is no significant advantage of increasing the drift doping zones beyond three. The use of multizone doping also resulted in the decrease of kink effect in the output characteristics of the proposed devices at low collector-emitter voltage (V_{CE}). This is due to the lowering of electric field at base-drift region (DR) junction. An improvement in tradeoff