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Ferroelectric Schottky barrier tunnel FET with gate-drain underlap: Proposal and investigation

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ABSTRACT

In this paper, for the first time, a novel ferroelectric schottky barrier tunnel FET (Fe SB-TFET) is proposed and investigated. The Fe SB-TFET consists of ferroelectric gate stack with highly doped pocket at the source/drain and channel interface. In addition, for the suppression of ambipolar leakage current (I_{AMB}), gate-drain underlap is employed. By using ferroelectric gate stack, we effectively amplified the applied gate voltage to enhance electric field for the reduction of tunneling barrier width at the source side schottky barrier. As a result, the increased tunneling probability improves the device performance in terms of high I_{ON}, high I_{ON}/I_{OFF} ratio, reduced I_{AMB} and low subthreshold swing (SS) as compared to the conventional SB-TFET having double pocket. We also investigate the influence of highly doped pocket (HDP) doping concentration and length on the device performance.

1. Introduction

Recently, Schottky barrier tunneling FETs (SB-TFETs) have gained much attention as a potential candidate for mixed-mode applications [1–3]. It offers several advantages, including low static source/drain resistance, low thermal budget and increased immunity to process variation [3–8]. However, the low I_{ON} because of large tunneling resistance is a major problem with this device [4]. Also, in the off-state, SB-TFET suffers from increased I_{AMB} due to ambipolar conduction [9–11]. In few reported study [1,3,4], to improve the overall device performance, highly doped pocket at the source end (Source pocket), drain end (Drain pocket) and both the ends (Double pocket) have been introduced. Among the above-mentioned device structures, SB-TFET with double pocket achieves improved performance as compared to other two device structures. However, the SB-TFET with double pocket as reported in Ref. [4] using SiO_2 as a gate oxide still suffer from low I_{ON} due to intrinsic channel region.

In this paper, in order to improve the I_{ON} and SS of the device, we proposed a novel Fe SB-TFET structure using 2D simulations, which uses ferroelectric stacked gate oxide in place of conventional SiO_2. Moreover, using gate-drain underlap, I_{AMB} has also been suppressed in the device. The Fe SB-TFET combines the principles of ferroelectric gate oxide and gate modulated Schottky barrier tunneling to improve the device performance. The ferroelectric gate oxide results negative capacitance effect which amplify the applied gate voltage that causes increased electric field at the source–channel junction. As a result, enhanced band bending reduces tunneling barrier width for electron injection. Accordingly, the DC performance of the device

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is improved. Using calibrated simulations, it has found that there is significant improvement in I_{ON}, I_{ON}/I_{OFF}, SS and reduction in I_{AMB} of the device as compared to the conventional SB-TFET. In addition, the influence of HDP doping concentration and length on the device performance is also investigated.

2. Device structure, simulation methodology and operating principle

2.1. Device structure

Fig. 1(a) and (b) shows the device structures of the conventional SB-TFET and the proposed Fe SB-TFET, respectively. The design parameters for the conventional SB-TFET with double pocket used in simulation are: channel doping concentration (p-type) $= 1 \times 10^{15}$ cm^{-3}, Si channel thickness (T_{si}) $= 10$ nm, buried oxide thickness (T_{box}) $= 20$ nm, highly doped pocket (HDP) concentration (n-type) $= 5 \times 10^{19}$ cm^{-3}, HDP length $= 2$ nm, and for the formation of Schottky source/drain, NiSi having electron Schottky barrier height (SBH) of 0.65 eV and hole SBH of 0.47 eV is considered [7]. All the design parameters for the proposed Fe SB-TFET are same as given above. In addition, gate stack of the proposed device is consists of high-k gate oxide (HfO_2) of EOT $= 1$ nm with a thin aluminum metal layer over it and ferroelectric oxide of PbZrTiO3 (PZT). The thin metallic layer eliminates the charge non-uniformity between the high-k gate oxide and ferroelectric oxide. The gate metal of length (L_g) 30 nm is also deposited over the ferroelectric oxide. The metal gate work function of Fe SB-TFET and conventional SB-TFET is 4.45 eV. Moreover, in Fe SB-TFET, gate-drain underlap length (L_{un}) of 15 nm is used. While the full gate length (L_g) and gate oxide thickness of the conventional SB-TFET is kept at 45 nm and 1 nm respectively. The equivalent capacitance model of the Fe SB-TFET is shown in Fig. 1(c), where C_{fe} represents the capacitance of the ferroelectric oxide layer and C_{ox} is the oxide capacitance. Also, C_s is the semiconductor capacitance comprises of the depletion capacitance, source to channel capacitance and drain to channel capacitance.

2.2. Simulation methodology

The device structures of conventional SB-TFET and the proposed Fe SB-TFET shown in Fig. 1(a) and (b) respectively, are simulated using two-dimensional Silvaco ATLAS simulator [12]. Universal schottky tunneling model based on WKB approximation is used to account schottky tunneling current through the Schottky barrier [4,12]. Lombardi mobility model and SRH model are also considered in simulations. Model calibration has been performed using published results in Ref. [3]. To model the ferroelectric effects of PZT, ferro model is incorporated in the simulation [12]. The ferroelectric properties of a FE material is determined by three parameters: the remnant polarization (P_r), the saturation polarization (P_s), and the coercive field (F_c). The values of the parameters used in simulation are: $P_r = 0.5 \times 10^{-6}$ C/cm^2, $P_s = 1 \times 10^{-6}$ C/cm^2, and $F_c = 1 \times 10^5$ V/cm, respectively. The device structure of proposed Fe SB-TFET is justifies using a 1-D landau model.

2.3. Operating principle

In conventional SB-TFET, carrier transport across the Schottky barrier is based on gate controlled Schottky barrier tunneling [3,4]. The applied gate voltage modulates the Schottky barrier at the source–channel junction by enhancing the electric field for changing the tunneling barrier width and available density of states [1,3]. In this device, the tunneling current is a function of SBH at the source-channel interface, gate oxide thickness and applied gate voltage [1]. For high SBH, I_{ON} and SS of the device is degraded due to large tunneling resistance at the source/drain and channel junction [1]. In addition, in the

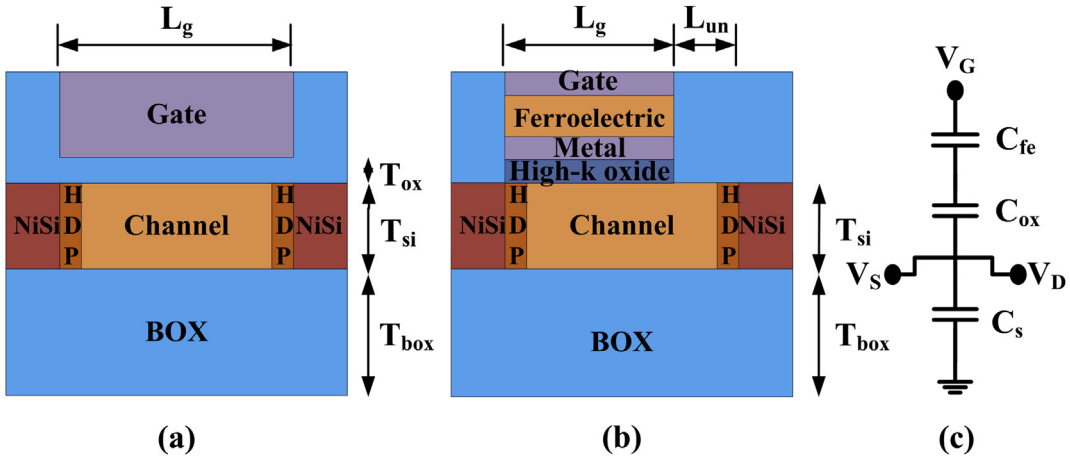

Fig. 1. Cross sectional view of (a) conventional SB-TFET, (b) the proposed Fe SB-TFET with gate-drain underlap and its equivalent capacitance model in (c).