Superlattices and Microstructures 89 (2016) 329–335

Contents lists available at ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Influence of hole and electron trapping on gate field dependent mobility and its degradation in organic field effect transistors

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ARTICLE INFO

Article history:
Received 25 October 2015
Received in revised form 23 November 2015
Accepted 24 November 2015
Available online 28 November 2015

Keywords:
OFET
Gate field dependent mobility
Degradation
Hole and electron trap concentration

ABSTRACT

Influence of hole and electron trapping effect on the gate field dependence of mobility, especially degradation at higher gate voltages, in organic field effect transistors is identified. Extent of mobility degradation was found to be dependent on the starting value of the gate voltage sweep. Both electron and hole trap concentrations are found to cause degradation in mobility with the former dominating over the latter. Significant increase in hole trap concentration causes slow increase in mobility for a certain span of gate voltage before shifting the onset point of degradation to much higher gate voltages. The interplay between the trap density, carrier density, mobility and the effective gate field decides the extent of degradation. Reduction of both hole and electron trap concentration by passivating the trap centres on the dielectric surface with suitable polymers resulted in constant mobility at higher gate voltages.

1. Introduction

Organic field effect transistors (OFET) are gaining worldwide importance due to their potential applications in flexible display devices, radiofrequency identification tags etc. Inspite of its growing importance, OFETs still suffer from low carrier mobility as compared to the conventional silicon based devices. OFET research community has employed many methods to improve charge carrier mobility. In all these studies charge carrier mobility in organic field effect transistors (OFETs) is generally extracted either in the linear or saturation regions using standard equations applied for silicon based FETs which has been a controversial issue [1] as these methods assume constant or average mobility respectively. Mobility is reported to be independent of gate voltage for single crystal organic semiconductors, as in ideal FETs [2], while in the case of polycrystalline and disordered materials, absence of well defined delocalized bands and presence of large density of localized states within the band gap result in mobility being very sensitive to gate voltage [1,3–7]. Dimitrakopoulos et al. explained gate field dependence of mobility using Multiple Trap and Release (MTR) model relating movement of Fermi level of semiconductor with gate voltage towards the delocalized mobility band edge during which recurrent trapping into localised traps above the mobility edge followed by thermal release into delocalized states below the same causes increase in mobility [3]. Variable Range Hopping (VRH) model connects hopping among an exponential distribution of localized states with a variable range [6,8]. While focus of many studies has been generally on the increase in mobility with gate voltage at low voltages, less

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http://dx.doi.org/10.1016/j.spmi.2015.11.030
0749-6036/

attention is paid on the behaviour of the same at higher gate voltages where it exhibits saturation or degradation [5,9–12] and hence more studies are required in this direction.

It is a common knowledge that for *p*-channel OFETs, hole and electron trapping occur significantly influencing many parameters like threshold voltage, parasitic contact resistance as well as charge carrier mobility. Though hole trapping is correlated with increase in mobility at low gate voltages for *p*-channel OFETs, to our knowledge, studies on the effect of the same and electron trapping on mobility degradation at higher gate voltages is negligible [13,14]. Bolsee et al. have mentioned about overall change in total mobility with electron detrapping, but have not discussed about gate voltage dependence [14]. In the present study, we have focused mainly on the dependence of mobility at higher gate voltages for *p*-channel OFETs and have identified major roles played by hole and electron traps in the same. The various experimental parameters like active layer thickness, moisture and oxygen in the ambient conditions etc. were found to influence hole and electron trap concentrations [15,16], the influence of these parameters on the gate field dependent mobility are investigated. We have also further shown that modifying the surface of SiO_2 dielectric with non polar polymers like polystyrene (PS), which offers hysteresis free behaviour for CuPc based OFETs [16,17], leads to negligible degradation. Since modifying with self assembled monolayers like octadecyltrichlorosilane (OTS) is also a common method employed [17], and was found to result in larger number of grain boundaries in CuPc films, effect of the same on gate field dependent mobility was also verified.

2. Experimental

n type Silicon (100) (0.01–0.015 Ωcm resistivity) was used as substrate with 200 nm thermally grown SiO_2 layer above it acting as dielectric. Copper phthalocyanine (CuPc), purchased from Sigma Aldrich and used as received, was thermally evaporated above the SiO_2 layer at a pressure of 1×10^{-5} mbar. Evaporation rate was maintained at 0.5–1 Å/s while thickness of the film for most part of the study was about 30 nm, as measured by quartz crystal monitor. The substrates were maintained at room temperature during the deposition of CuPc. For studying the effect of active layer thickness, CuPc films of thicknesses 7.5, 15, 70 and 100 nm were also deposited [15]. For polymer modification of SiO_2 dielectric, a 70 nm thick film of polystyrene (PS) was deposited above the SiO_2 layer by spin coating 2 wt. % solution of PS in toluene at a speed of 4000 rpm for 1 min. PS film was further cured under vacuum at 60 °C for 4 h to remove the residual solvent. For modification with self assembled monolayer (SAM) of octadecyltrichlorosilane (OTS) molecules, Piranha cleaned SiO_2 substrates were immersed in a freshly prepared 0.5 mM OTS solution in toluene for 24 h, in an argon gas filled glove box (O_2, RH < 1 ppm) [16]. Gold films for source (*S*) and drain (*D*) electrodes were thermally evaporated through a shadow mask above CuPc films with channel length (*L*) and width (*W*) of 25 μm and 2 mm respectively. Surface morphology of CuPc films were verified using Atomic Force Microscopy (AFM) (NT-MDT). Water drop contact angle on unmodified as well as PS and OTS modified SiO_2 were measured using DATA Physics contact angle metre. The current–voltage (*I–V*) characteristics were measured in air at room temperature using Keithley voltage source current metre, (model 6487). Most of the measurements were carried out under normal room light conditions unless specified.

3. Results and discussion

3.1. Structural characterisation

Contact angle of unmodified SiO_2, PS and OTS modified SiO_2 were measured to be <10, 90 and 107° respectively indicating the change in nature of SiO_2 surface from hydrophilic to hydrophobic in nature. This indicates passivation of OH groups on SiO_2 surface. AFM imaging revealed variation in grain sizes on the surface modified dielectrics as well as with different thickness of CuPc film (Fig. 1) [15,16]. Large number of grain boundaries with grain size much smaller than that of 30 nm film on unmodified SiO_2 is observed for 7.5 nm film (Fig. 1d) as well as that on OTS/SiO_2 (Fig. 1c). On PS modified SiO_2 grains appear more interconnected with less grain boundaries (Fig. 1b). Grain size increased to above 350 nm for 100 nm thick film (Fig. 1f).

3.2. Electrical characterization

Typical transfer characteristics of OFETs with 30 nm thick CuPc film on SiO_2 dielectric are shown in Fig. 2a, where gate voltage (V_G) is scanned from −4 and from +20 V, with drain voltage fixed at −50 V corresponding to the saturation region. The $\sqrt{I_D}$ *vs* V_G plot shows a clear downward curvature at higher negative V_G for scan from +20 V and a more close to ideal FET characteristics for that from −4 V, indicating influence of the starting voltage of the scan on gate field dependent mobility.

Charge carrier mobility has been estimated from $\sqrt{I_D}$ *vs* V_G plots using equation (1) [16].

$$I_D = (WC_i/2L)\mu(V_G - V_T)^2 \quad (1)$$

Though equation (1) is valid mainly for average mobility, it can be used to a first approximation to estimate gate field dependent mobility from the slope at every V_G [10,12,18,19]. Fig. 2b shows the V_G dependent mobility plots for scans from −4 and +20 V which are used as reference throughout this study. To compare the extent of degradation depending on the starting