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Upper drift region double step partial SOI LDMOSFET: A novel device for enhancing breakdown voltage and output characteristics

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ABSTRACT

A new LDMOSFET structure called upper drift region double step partial silicon on insulator (UDDS-PSOI) is proposed to enhance the breakdown voltage (BV) and output characteristics. The proposed structure contains two vertical steps in the top surface of the drift region. It is demonstrated that in the proposed structure, the lateral electric field distribution is modified by producing two additional electric field peaks, which decrease the common peaks near the drain and gate junctions. The electric field distribution in the drift region is modulated and that of the buried layer is enhanced by the two steps in the top surface of the drift region, thereby resulting in the enhancement of the BV. The effect of device parameters, such as the step height and length in the top surface of the drift region, the doping concentration in the drift region, and the buried oxide length and thickness, on the electric field distribution and the BV of the proposed structure is studied. Simulation results from two-dimensional ATLAS simulator show that the BV of the UDDS-PSOI structure is 120% and 220% higher than that of conventional partial SOI (C-PSOI) and conventional SOI (C-SOI) structures, respectively. Furthermore, the drain current of the UDDS-PSOI is 11% larger than the C-PSOI structure with a drain-source voltage $V_{DS} = 100$ V and gate-source voltage $V_{GS} = 5$ V. Simulation results show that R_{on} in the proposed structure is 74% and 48% of that in C-PSOI and C-SOI structures, respectively.

1. 1Introduction

Silicon on insulator (SOI) technology has attracted much attention in power integrated circuits in the last decade. SOI technology has numerous advantages over bulk silicon technology, such as ideal device isolation [1], reduced parasitic capacitance, excellent sub-threshold slope, elimination of latch up [2], increased switching speed, radiation hardness [3], and reduced leakage current [4]. Also, the lateral double diffused MOSFET (LDMOS) on SOI substrate has been widely used in intelligent power applications because of the ease of implementing low voltage CMOS signal processing circuits in conjunction with high-voltage LDMOS drivers on the same chip. It also is compatible with the VLSI process and is easy to integrate with other processes [5]. However, SOI power devices suffer from a low vertical breakdown voltage (BV) and the self-heating effect (SHE). The vertical BV of the conventional SOI (C-SOI) is limited by the SOI layer and the buried oxide (BOX) layer, leading to the difficulty in achieving a high voltage in C-SOI structures. The drift region of LDMOS in the SOI technology

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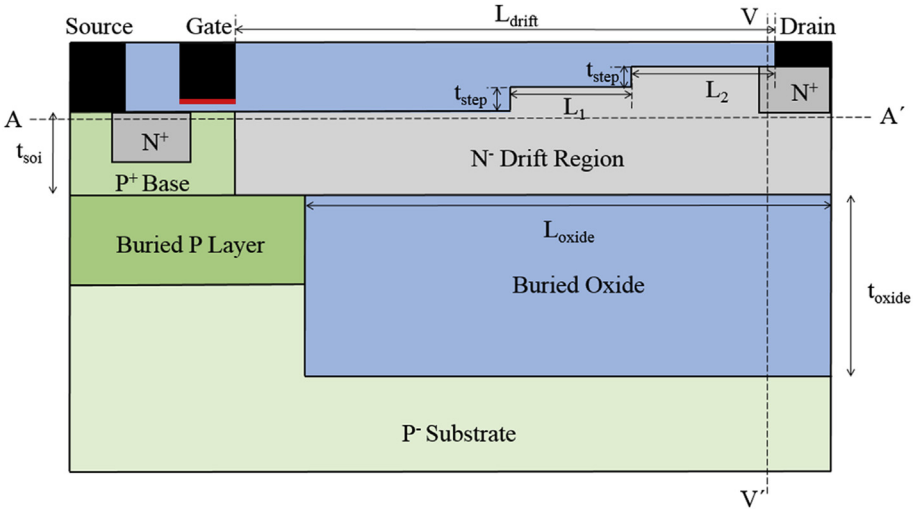

Fig. 1. A schematic cross section of the UDDS-PSOI structure.

is sandwiched between the field oxide and thick oxide. Hence, considerable heat generated in the SOI devices in power applications cannot dissipate in time, leading to a much higher temperature than bulk silicon devices due to the low conductivity of the oxide. This SHE results in reduced carrier mobility, decreased transconductance, deteriorated reliability and a threshold voltage shift. Various LDMOS structures have been proposed to enhance the BV and reduce the SHE [6–12]. One example is partial SOI (PSOI) [13–26]. The thin SOI LDMOS devices based on this technology have a buried oxide etched underneath the drain to open a silicon window. Thus the SHE is drastically reduced since heat can now dissipate through the silicon window to the substrate. Moreover, the presence of the silicon window allows the temperature to distribute more evenly along the drift region, eliminating the formation of localized hot spots in the vicinity of the source terminal. Also the electric field can extend to the substrate through the window which is created by PSOI, resulting in the improvement of the vertical BV. There are two peaks in the lateral electric field distribution of thin-film SOI power devices: one near the gate/drift region junction and the other one near the drift region/drain junction [10,11]. A high BV can be provided by reducing either

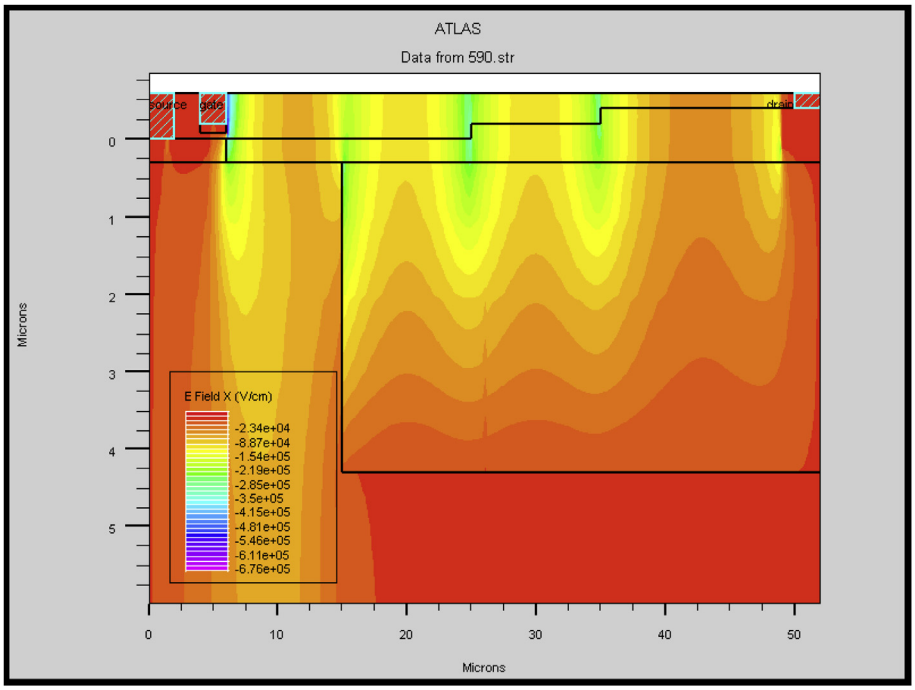

Fig. 2. Lateral electric field contours for the UDDS-PSOI structure.