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Review

A review of InP/InAlAs/InGaAs based transistors for high frequency applications

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ABSTRACT

This paper presents an overview of the rapid progress being made in the development of InP based devices for high speed applications. Over the past few decades, major aero space industries have been developing InP based hetero structure devices like hetero junction bipolar transistors (HBTs) and high electron mobility transistors (HEMT) because of their low DC power due to excellent low voltage operation and milli-meter wave frequency performance even though its widespread use has been limited by high cost. InP based HBTs, MOSFETs and HEMTs have also been developed by commercial companies for applications in high speed fiber optic communications because InP based device technologies takes advantage of the intrinsic material properties such as high thermal conductivity, high electron mobility and low energy band gap for low voltage operation compared to silicon, silicon–germenium, and GaAs based semiconductor devices.

Contents

1. Introduction

Indium Phosphide (InP) is a material system with potential applications in high speed electronics, satellite communications, critical semiconductor IC applications, high speed internet access, real time multimedia file transfer and video

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conferencing due to its high room temperature electron mobility, higher velocity of saturation and high sheet electron densities. There has been considerable interest in developing InP based transistors such as HBTs, MOSFETs and HEMTs using various technologies such as gate engineering, source/drain engineering and material engineering ever since some advantages of the intrinsic properties such as high electron mobility, high thermal conductivity and low voltage operation in order to gain advantages over GaAs, Silicon and SiGe based semiconductor technologies. Recent advances of InP based transistors with operating frequencies of several hundreds of gigahertz (GHz) [1,2] together with the outstanding intrinsic properties of the InP material system, make them attractive candidates for key components in critical IC applications even though its widespread use has been limited in applications with higher level of integration due to low process yield and thereby high cost [3].

The initial mobility enhancement techniques (MBE, Hetero structures) that were observed were quite modest at room temperature but much more significant at low temperatures. Over time, the low temperature mobility would dramatically improve leading to fundamental discoveries in solid state physics [4]. This paper traces the most significant steps of the evolution of the indium phosphide based MOSFETs, HBTs and HEMTs from their inception to its current state in various semiconductor systems. It also outlines some of the new inventions such as the development of ultra low-noise InP/InAlAs/InGaAs high-electron mobility transistors (InP HEMTs) optimized for operation at 10 K (cryogenic) enabled in solid-state physics. This review is finished by sketching a future for new applications for InP based HBTs and HEMTs in several domains.

2. High-κ dielectrics for high speed devices

To achieve higher density, lower power consumption and high performance, silicon (Si) complementary metal-oxide-semiconductor (CMOS) devices have been scaled for more than 40 years. As CMOS scaling is approaching the physical and optimal limits [5,6], future scaling of CMOS in accordance with Moore's law and to meet the demands of the ITRS (International technology roadmap for semiconductors) roadmap will require new materials for the gate dielectrics [7–9] and the high mobility channels [10–12] as well as innovative structures [13,14]. In the past, the ability to reap the benefits of the outstanding transport properties of the III–V compound semiconductors for use in the n-channel devices has been limited by the lack of high quality stable oxides that enhance the gate oxide–semiconductor interface thermodynamically [15–19]. The power consumption of any devices depends on two factors namely off current (I_{off}) and supply voltage (V_{DD}). The off current, I_{off}, consist of subthreshold leakage, gate induced drain leakage (GIDL) and gate leakage [20,21]. In summary, to obtain a semiconductor device with low power consumption and high performance, a high on current (I_{on}), a low off current and a small supply voltage are required [22]. In recent years, there has been increasing interest in InP based hetero structure MOSFETs with high mobility InGaAs channel. Applying oxides with high dielectric constant (high-κ) instead of SiO_2 as the gate oxide on III–V materials can reduce the gate leakage current at the same EOT, thus reduces the power consumption [23,24]. The properties of some of the high-κ materials are given in Table 1.

In recent years, the surface-channel inversion-mode III–V MOSFETs [25] with atomic layer deposited (ALD) [26–38] Al_2O_3, HfO_2, HfAlO, ZrO_2 or $LaAlO_3$ dielectrics [39–51] molecular beam epitaxy (MBE) $Ga_2O_3(Gd_2O_3)$ dielectrics [52–56] and Si, Ge, Si_xN_y, Ge_xN_y, or Al_xN_y interfacial passivation layer (IPL) and high-κ gate stacks [57–61] show promising results. The various interface treatment techniques reported in the past years such as sulfur (S) compounds [62], nitrogen plasma [60], hydrogen bromide solution [63], PH_3 passivation [64], and fluorine treatment [65,66] have very much improved the device characteristics. On the other hand, buried channel III–V MOSFETs [67–69] with InAlAs barrier layer and Si interfacial passivation layer [70,71], or with single InP barrier layer or InP/InAlAs double barrier layer using ex-situ ALD oxide [72,73], or flat band InGaAs MOSFETs with GaAs/AlGaAs barrier layer and Si δ-doping using in-situ MBE $GaGdO_x$ gate oxide [74–79], or Metal oxide semiconductor-high-electron mobility transistors (MOS-HEMTs) [76] have been demonstrated much higher channel mobility [70–76] compared to surface channel MOSFETs [39–55]. Also the gate leakage current density of buried channel InGaAs MOSFETs [56–58] can be several orders of magnitude lower than HEMTs [77,78].

A high performance enhancement-mode planar InGaAs MOSFETs feature a composite gate insulator ($InP/Al_2O_3/HfO_2$) has been successfully demonstrated using a three-step recess fabrication process [80,81]. The composite high-κ gate stack enables both (i) thin electrical oxide thickness (t_{OXE}) and low gate leakage (J_G) and (ii) effective carrier confinement and high effective carrier velocity (V_{eff}) in the Quantum Well (QW) channel [82]. In summary, the $In_{0.53}Ga_{0.47}As$ n-MOSFETs with different gate dielectrics (Al_2O_3, HfO_2 and $LaAlO_3$) deposited by ALD, or CVD [83] HfO_2 is demonstrated to have the best EOT

Table 1
High-κ materials and its properties.

Sl. No.	Properties	SiO_2	Al_2O_3	HfO_2	ZrO_2	La_2O_3
1	Dielectric constant	3.9	8–9	18–25	18–30	20–36
2	Band gap (eV)	9	8.8	6	5.8	4.3
3	Band offset for electrons (eV)	3.5	2.8	1.5	1.4	2.3
4	Band offset for holes (eV)	4.4	4.9	3.4	3.3	0.9