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Impacts of virtual substrate doping on high frequency characteristics of biaxially strained Si PMOSFET

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ABSTRACT

Formation of a parasitic channel in biaxially strained Si channel p-MOSFET, degrades performance of the device. In this paper the effect of SiGe (virtual substrate) doping on formation of parasitic channel and high frequency characteristics of the strained MOSFET has been studied. Simulation results, indicate that increasing virtual substrate's doping from e.g. $4 \times 10^{15}\,cm^{-3}$ to $4 \times 10^{17}\,cm^{-3}$ effectively eliminates parasitic channel by reducing hole concentration from $1 \times 10^{17}\,cm^{-3}$ to $1 \times 10^{11}\,cm^{-3}$ in the parasitic channel. This improves MOSFET's characteristics including parasitic capacitances and channel length modulation. Also it has been demonstrated that the highest unity-gain bandwidth might be achieved at doping level of $4 \times 10^{17}\,cm^{-3}$.

1. Introduction

Strain has been one of the promising candidates when semiconductor industry faced red brick walls while trying to follow the Moore's law [1]. It has been shown that biaxial strain in Si enhances the carriers' mobility and improves the MOSFET current [2–4]. However, biaxially strained Si

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p-MOSFET, faces a major drawback. In conventional strained p-MOSFET structure formation of a quantum well (QW) within SiGe layer (virtual substrate), confines holes inside this layer [5]. This provides a low resistance parasitic channel inside SiGe layer close to the Si/SiGe interface which is parallel to the main channel in the strained Si. This parasitic channel increases MOSFET's drain current. However a significant portion of the current flows through the parasitic path and is not controlled entirely by the gate voltage. This effect degrades MOSFET's high frequency characteristics e.g. parasitic capacitors.

Rim et al. [6] proposed to add a graded SiGe layer between strained Si and relaxed SiGe. This approach provides a smooth band energy variation between strained Si and relaxed SiGe and removes the parasitic channel. However, the thick strained layer used in this method makes fabrication process more complicated. It also partially relaxes the strain in the Silicon channel and therefore decreases channel mobility, which was the main motivation for switching to strained Si devices. Sugii et al. [7] proposed another approach based on highly doped bottom side of the strained Si layer to eliminate the parasitic channel. However, fabrication process of the highly doped structure involves ion implantation and a subsequent annealing step, which results in considerable number of defects in the strained Si channel and degrades mobility of the devices.

Chandrasekaran et al. [8] have reported formation of parasitic channel in substrate QW as a "plateau" in *C–V* characteristics of a MOS capacitor structure. Although they have shown that increasing SiGe doping removes this plateau, impact of this method on the other MOSFET characteristics has not been investigated. In this work, we have studied the impact of parasitic channel under various substrate doping levels on high frequency characteristics of the p-MOSFET. In this approach, virtual substrate is being doped during the SiGe deposition process which results in lower defect density in contrast to ion implantation. Also this approach does not increase the strained layer thickness.

2. Structure

Fig. 1 shows a schematic cross section view of the biaxially strained Si p-MOSFET. The structure consists of a thin Si layer (15 nm) which has been grown by epitaxy on top of a thick, fully relaxed n-type SiGe which is called "virtual substrate". The relaxed SiGe layer should be grown on a graded SiGe layer to be fully relaxed [9]. The channel length is 100 nm with uniform n-type doping concentration of 4×10^{17} cm^{-3}, Si lattice orientation is (100), and the gate is made of p-type poly Silicon. Due

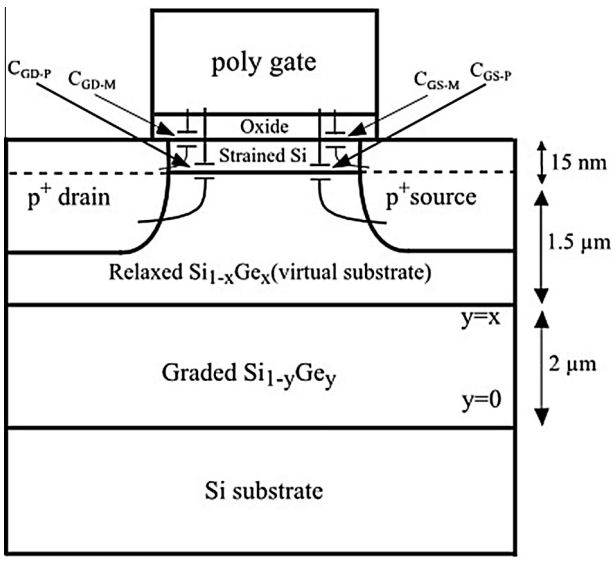

Fig. 1. Schematic cross section view of a biaxially strained p-MOSFET.