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Improved performance of 4H–SiC MESFETs with Γ-gate and recessed p-buffer layer

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An improved 4H–SiC MESFET with Γ-gate and recessed p-buffer layer (ΓRP-MESFET) is proposed in this paper. The channel electric field and the gate depletion layer have been modulated by utilizing Γ-gate and introducing recessed p-buffer layer simultaneously in the ΓRP-MESFET structure. The simulated results show that the drain saturation current and the breakdown voltage of the proposed structure are about 18.5% and 19.4% larger than those of the double recessed structure (DR-MESFET), respectively. Therefore, the maximum output power density of 8.17 W/mm can be achieved, which is about 42% higher than that of the reported one. The cut-off frequency (f_T) of the proposed structure is 19.8 GHz, which is higher than that of the conventional structure due to its smaller gate–source capacitance (C_{gs}).

1. Introduction

SiC based metal semiconductor field effect transistor (MESFET) is considered to be a potential candidate for high power, high efficiency and high frequency microwave applications [1,2]. For 4H–SiC MESFET, it is critical to sustain large drain saturation current (I_{dsat}) and maintain high breakdown voltage to obtain high maximum output power density (P_{max}). Many new techniques and magnificent works have been done to obtain a significant improvement in device breakdown voltage due to the electric field modulation by modifying the channel [3–5]. To allow for high drain current, a larger product of the channel doping and thickness ($N \times a$) is required. However, a higher channel doping or a thicker channel layer will lead to lower breakdown voltage (V_b) and DC transconductance (g_m) [6,7]. The fact has been demonstrated in many literatures that the region under gate has a prominent influence on drain current [8–10]. The trade-off among I_{dsat}, V_b and g_m is a difficult problem, and a potential way to improve them is still worth investigating for high power applications. To obtain better DC and RF characteristics, the challenge addressed in this paper is to change the location and shape of gate and recessed p-buffer layer.

In this paper, a novel 4H–SiC MESFET with Γ-gate and recessed p-buffer layer (ΓRP-MESFET) is proposed. The new structure is based on the double-recessed structure (DR-MESFET) which mainly contains upper and lower gates [11], but the location of upper and lower gates relative to the channel surface is changed. The upper one supports wider channel and allows higher drain current. The electric field crowding at upper gate corner near drain is reduced due to the electric field modulation, thus improving the breakdown voltage. To keep the channel controlled by the gate bias effectively, the distance between lower gate and the bottom of channel remains unchanged by utilizing recessed p-buffer layer, since the g_m is very

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important parameter as it indicates the driving capability of the device. The unique features of the proposed structure are explored in detail and compared with those of the DR-MESFET structure in terms of drain current, breakdown voltage, gate–source capacitance, transconductance and small-signal high frequency characteristics.

2. Device structure

Schematic cross-sections of the DR-MESFET and ΓRP-MESFET structures are presented in Fig. 1a and b, respectively. The dimensions of the proposed structure are as follows: gate length $L_g = 0.7$ μm, gate–drain spacing $L_{gd} = 1$ μm, gate–source spacing $L_{gs} = 0.5$ μm. The channel regions from source side and drain side to gate are both etched 0.05 μm for the channel recessed device. The channel thickness is 0.25 μm and channel doping $N_D = 3 \times 10^{17}$ cm^{-3}. The doping concentration and thickness of the p-buffer layer are 1.4×10^{15} cm^{-3} and 0.5 μm, respectively. The recessed p-buffer layer depth into channel and length are 0.05 and 0.35 μm, respectively. The doping concentration of source and drain cap layers is 2×10^{19} cm^{-3}. Nickel is chosen for the gate Schottky contact with a work function of 5.1 eV. The devices are simulated by using two-dimensional ISE-TCAD simulation software with 4H–SiC material parameters. A temperature of 300 K is employed in the simulations.

3. Results and discussion

3.1. DC characteristics

Fig. 2 shows the simulated drain current (I_d) versus the drain-source voltage (V_{ds}) for the DR-MESFET and ΓRP-MESFET structures as a function of gate voltage bias (V_{gs}) from 0 to −9 V with a step of −3 V. It can be seen that the drain current of the ΓRP-MESFET structure is larger evidently at various V_{gs} than that of the DR-MESFET structure. That is because the gate depletion layer distribution of the ΓRP-MESFET structure is changed since the higher upper gate modulates the channel transversal electric field, and the gate depletion layer in channel is less than that of the DR-MESFET structure. Since the drain current is in direct proportion to the channel doping and dimensions ($N \times a$), the region relative thickness under gate of the ΓRP-MESFET structure is wider and therefore the drain current will increase rapidly. The maximum drain saturation current of the ΓRP-MESFET structure is 531 mA/mm at $V_{gs} = 0$ V in comparison with 448 mA/mm of the DR-MESFET structure.

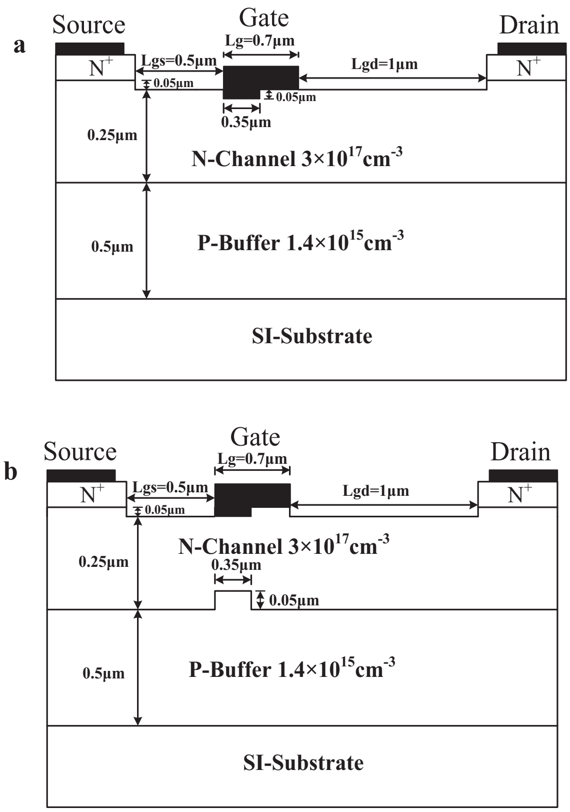

Fig. 1. Schematic cross-sections of the (*a*) DR-MESFET and (*b*) ΓRP-MESFET structures.