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Controlling floating body effect in high temperatures: L-shape SiGe region in nano-scale MOSFET

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ABSTRACT

In this paper a new technique for controlling floating body effect and self-heating effects is proposed. The main idea in the proposed structure is using a L-shape SiGe region in the nano-scale SOI-MOSFET (LS-SOI). The L-shape SiGe region is located in the source region and is extended under channel. The difference band gap between silicon and silicon–germanium cause discontinuity in band diagram which helps to collect channel holes. Reducing the hole density in channel of the proposed LS-SOI in comparison to conventional SOI-MOSFET (C-SOI) results in suppressed floating body effect. Also, the SiGe region under the channel decreases the lattice temperature in the LS-SOI. Replacing the SiGe with higher thermal capability than buried oxide is useful to have a reliable structure. Moreover, effective mobility, off current and sub-threshold swing improves in the proposed structure.

1. Introduction

Silicon-on-insulator (SOI) MOSFETs are preferred devices in nano-technology due to their low power consumption and high speed performance [1]. Beside the advantages of buried oxide (BOX), this insulator layer causes two important drawbacks in such devices. The first one is floating body effect and the other is self-heating effect [2–4].

In a partially depleted (PD) MOSFET the bottom region of the silicon under the channel is floating. In other words the buried oxide isolates channel region from the substrate that generates accumulation of holes by the impact ionization. This condition causes low breakdown voltage, kink effect, high subthreshold slope and so on [5–7]. There are two main solutions for controlling floating body effect. The first one is providing body contacts [8] and the second solution is using semiconductor materials with different band gap in the device [9]. Using body contact not only suffers from an area penalty but also reduces hole absorption mechanism with increasing channel width. In the second solution, a band gap narrowing of the source region absorbs the hole accumulations. Using SiGe material which has narrower band gap than silicon is common in the MOSFET devices. In this paper a L-shape SiGe region is considered in the SOI-MOSFET structure to control floating body effect and also reduce lattice temperature. This L shape SiGe region is considered in part of source region and extended in the buried oxide under the channel region. The name of the proposed structure is L shape SiGe region in SOI-MOSFET (LS-SOI) which is simulated with ATLAS simulator and compared with conventional SOI-MOSFET without any SiGe region [10]. It is important to note that the exact value of the SiGe region in the source and buried oxide of the LS-SOI is determined with the simulation.

In another vision, the L-shape SiGe region controls self-heating effect and reduces lattice temperature. This effect is due to the extending SiGe region under the channel. Replacing a semiconductor material instead of insulator layer is attractive to

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achieve reliable devices [11–13]. So, the proposed structure could control floating body effect and has desirable behavior in high temperature. Furthermore, the proposed transistor shows acceptable behavior in terms of drain current, mobility, subthreshold slope, leakage current and lattice temperature.

The rest of the paper is organized as follows: after introducing the proposed device structure in Section 2, the simulation results for the proposed structure using ATLAS simulation are organized in Section 3. Section 4 concludes the results.

2. Device structure and mechanism

The schematic of the proposed L shape SiGe region in SOI-MOSFET (LS-SOI) is illustrated in Fig. 1. As the figure shows, the length of SiGe region in the source is determined with L_{SiGe}. Also, the SiGe region which is extended under the channel has $L_{SiGe} + L_{ch}$ length. The thickness of SiGe region (t_{SiGe}) is divided into two parts: the thickness of SiGe in the source is labeled with t_1 and its thickness in the buried oxide has t_2 symbol. The exact values of these thicknesses and lengths are defined in the next section to control floating body effect and also have acceptable lattice temperature and gate-substrate capacitance. Moreover, the device parameters for the LS-SOI used in the simulation are listed in Table 1.

In the simulation, drift diffusion approach is used [14] and the models are activated in simulation comprise of concentration dependent mobility, field dependent mobility, and velocity saturation model. The parameters in the model used from look up table are carriers mobility $\mu_{no} = 1076\ cm^2/V\ s$, $\mu_{po} = 460.9\ cm^2/V\ s$, and $\tau_n = \tau_p = 1 \times 10^{-7}$ s are the electron and hole lifetimes. Also, suitable empirical β_n, β_p are chosen to calibrate the drift diffusion transport model [15].

Physical models accounting for temperature and electric field dependence of mobility are considered in the simulation. Also, Shockley–Read–Hall [16,17] and Auger recombination models are included for minority carrier recombination. Moreover, the inversion-layer Lombardi mobility model is used to calculate the mobility degradation which occurs due to higher surface scattering near the semiconductor–insulator interface. The impact ionization and band-to-band Augur recombination models are considered in the simulation.

3. Results and discussion

3.1. Floating body effect

Floating body effect generates excess holes in the channel. In SOI technology, theses holes could not flow to the substrate and make a lot of problems in the device. A clear effect of excess holes in the channel illustrates in the output characteristic of the SOI-MOSFET. Fig. 2 compares the drain current of the proposed LS-SOI and C-SOI structures. A sudden rise in the saturation region of the C-SOI is identified as a kink effect, because the body is floating. In the proposed structure, floating body effect is controlled. The N-SiGe region in the source and under the channel has hetro-structure that makes a discontinuity in the band diagram of the P-channel and N-SiGe. As Fig. 3 shows, the band gap difference is seen as discontinuity in the

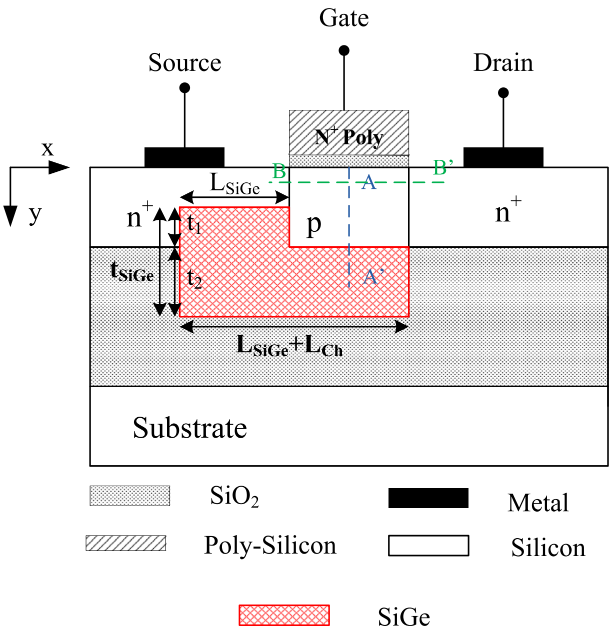

Fig. 1. A schematic view of the L-shape SiGe region in the SOI-MOSFET (LS-SOI).