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High performance strained $Si_{0.5}Ge_{0.5}$ quantum-well p-MOSFETs fabricated using a high-κ/metal-gate last process

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ABSTRACT

A high-κ/metal-gate (HKMG) last process for fabricating strained $Si_{0.5}Ge_{0.5}$ quantum-well (QW) p-channel metal oxide semiconductor field effect transistors (p-MOSFETs) is presented. Because the HKMG was formed after the ion-implant doping activation process, the thermal budget issue could be mitigated. The transistor features good transfer and output characteristics with I_{on}/I_{off} ratio up to 10^6 and threshold voltage (V_T) down to 0.1 V. The effective hole mobility of the SiGe QW transistor reaches 215 $cm^2/V\,s$ for strong inversion conditions, which is 2.74 times the SOI device's hole mobility.

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1. Introduction

As semiconductor technology goes into a new era of nano-dimensions, Si metal oxide semiconductor field effect transistors (MOSFETs) are facing a lot of challenges. Higher carrier mobility and SiO_2/poly-Si gate stack replacement are two main issues, leading to introduction of novel high mobility channel and high-κ dielectric/metal gate (HKMG) stacks.

For p-channel MOSFETs, SiGe is regarded as the most promising channel material due to its intrinsic high hole mobility and easy integration within the existing sophisticated Si technology [1–3]. Si/SiGe/Si quantum-well (QW) p-MOSFETs have received great attention, because a thin Si cap layer provides a good high-κ/Si interface without degrading the hole mobility [4,5].

Various HKMG stacks integrated into SiGe QW p-MOSFETs have been reported [6–10]. However, the thermal stability of an HKMG during the conventional gate-first process is considered to be one of the fundamental limitations of HKMG integration. Many high-κ materials exhibit low crystallization temperatures, and the effective work function (EWF) of metal gate becomes unstable during the high temperature treatment [11,12].

In order to overcome these problems, a novel and practical HKMG-last process is developed to fabricate strained sSi/$Si_{0.5}Ge_{0.5}$/sSOI QW p-MOSFETs. In this process, Al_2O_3/TiN gate stack was deposited after source/drain (S/D) formation. The transistors are electrically characterized in terms of *I–V* performances and hole mobility.

2. Device fabrication

A biaxially tensely strained SOI (100) substrate with a 12 nm top sSi layer is used as the starting wafer. The tensile strain in the sSOI layer is $\varepsilon = 0.8\%$ ($\sigma = 1.35$ GPa), corresponding to a Ge content of 20% in the virtual SiGe substrate prior sSOI fabrication. A lightly p-doped $Si_{0.5}Ge_{0.5}$ layer was pseudomorphically grown with the thickness of 25 nm on sSOI substrate using reduced pressure chemical vapor deposition (RPCVD). The thickness of $Si_{0.5}Ge_{0.5}$ is below the critical thickness to avoid strain relaxation, corresponding to −2.1% biaxial compressive strain applied in the $Si_{0.5}Ge_{0.5}$ channel. The epitaxy of the SiGe layer was followed by the growth of 5 nm sSi cap layer, which confines the holes in the SiGe quantum-well. The sSi cap suppresses the hole scattering at the oxide/semiconductor interface and prevents SiGe oxidation.

P-type MOSFETs were fabricated with Al_2O_3/TiN gate stacks using a HKMG-last process. After mesa definition, the S/D implantation was carried out with a 10 keV BF_2^+ at a dose of 2×15 cm^{-2} followed by 600 °C rapid thermal annealing (RTP) for 1 min. The S/D ion implantation parameters and the activation temperature were chosen such that the SiGe layer fully conserves the strain both in the channel region and S/D regions. After S/D implantation, standard RCA pre-high-κ cleaning process was performed followed by high-κ and metal gate deposition. The Al_2O_3 gate dielectric was deposited by atomic layer deposition (ALD) to a thickness of 10 nm followed by sputter deposition of 20 nm TiN gate metal. Through this HKMG-last process, HKMG avoided the high temperature dopant activation treatment, so the high-κ Al_2O_3 dielectric was prevented from crystallization and the work function of the TiN metal gate kept stable. Finally, metal Al was deposited for electrical contacts. The final device structure of the transistor is schematically shown in Fig. 1.

3. Results and discussions

The *I–V* characteristics of strained $Si_{0.5}Ge_{0.5}$ QW p-MOSFET with Al_2O_3/TiN gate stack and a gate length $L = 10$ μm are shown in Fig. 2. The transistor presents an I_{on}/I_{off} ratio up to 10^6 and the output characteristics show a good current saturation. The gate stack induces a threshold voltage V_T of 0.1 V and no threshold voltage adjustment was made in our process. Thanks to the better thermal stability of the metal gate during the HKMG-last process, it can deliver higher EWF, thus V_T in this work is much lower than those of HKMG-first devices [6,7].

The *I–V* characteristics of a similar device but fabricated on fully depleted SOI substrate with 30 nm top Si are also plotted in Fig. 2 for comparison. The SiGe QW transistors show higher on-current than