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Highly efficient PWM synchronous buck converter with optimized LDMOS

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ABSTRACT

In this work, a design of high efficiency synchronous buck converter with an optimized LDMOS is presented which works in VHF frequency domain. The circuit performance of the buck converter is then analyzed and optimized to increase the efficiency and to reduce the power losses without modifying the circuit. The analysis and optimization is performed by varying the different device parameters like drift region doping concentration (D_{Drift}) and drift region length (L_{Drift}) along with the circuit level parameters like the dead time and the switching frequency. The effect of the parameters is found to reduce the power losses of the circuit. The circuit with optimized parameters yields 80% efficiency at 100 MHz switching frequency.

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1. Introduction

The rapid growth in wireless and mobile communication devices requires low power, high efficiency, small-sized power conversion systems that work in the VHF frequency domain [1]. Inclusion of RF analog processing unit consisting amplifiers, modulators and even power amplifiers on a system on chip (SOC) requires an accurate, cost effective, highly efficient power management system which occupies less area to minimize the leakage power [2,3].

DC to DC converters are good solution for a low power, small area power management system as they are easy to design even with low cost components and can be tailored to fit any requirement [4].

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For a battery driven handheld device primary criteria is high conversion efficiency [5] which can be provided by a conventional Pulse Width Modulated (PWM) converter only under large load at low switching frequency [6]. Over the years different circuit techniques have been developed [7–10] to improve the conversion efficiency at higher frequencies. High frequency operation of PWM converter demands small values of *R*, *L*, and *C* for easier integration with active silicon components. On the other hand, device cutoff frequency limits the range of operating frequency of the circuit restricting high frequency operations [11]. A great deal of research has been done for rectifying this problem and many techniques have been proposed to increase the range of operating frequency used for switching in PWM [12]. A non-classical device called Laterally Double-diffuse MOSFET (*LDMOS*) is a good alternative to deal with the low bandwidth problem [14] as it is having a high frequency of operation [13]. LDMOS have been investigated by many researches for its reliability under high frequency and high voltage operation and provides a high breakdown voltage [15–17]. These investigations provides basis for the effectiveness of LDMOS in the buck converter circuit designed here.

In this work, LDMOS is proposed as the replacement of the conventional devices [18] to make an efficient synchronous buck converter and mixed mode simulation of PWM synchronous converter are performed to optimize device performance for optimized conversion efficiency of the buck converter circuit.

2. Device structure and simulation method

In this section device structure and optimization of LDMOS is provided. Fig. 1 describes different parts of an N-channel LDMOS (*NLDMOS*). In the LDMOS the region between the source and the drain is divided into two parts, shown in Fig. 1, the left part is the P type doped channel region and the other part is the N type lightly doped drain (*LDD*) region or "the drift region" [19]. The two parameters that have been varied are the width of the device, the length of the drift region (L_{Drift}) and the doping of the drift region (D_{Drift}).

In this study the source length (L_{Soruce}) and drain length (L_{Drain}), used in the device is 1 μm with the channel length ($L_{Channel}$) of 1.5 μm and oxide thickness of 50 nm. Also, the Drain/Source doping is 10^{20} cm^{-3} and the channel doping is 10^{15} cm^{-3}.

The above described device is simulated and the drain current (I_D) vs. gate to source voltage (V_{GS}) and the I_D vs. drain to source voltage (V_{DS}) of the device is presented in Figs. 2 and 3. The gate length 2 μm, drift doping concentration 5×10^{15} cm^{-3}, drift length 5 μm are chosen.

Simulations for this work are done by 2D device simulator [20]. Field dependent mobility model is used to consider the carrier mobility [20]. This model considers the Caughey and Thomas expressions to model the mobility [21]. The Shockley–Read–Hall (SRH) recombination model is used to incorporate the recombination effect in the device. The impact ionization of the device is modeled with Selberherr's impact ionization model.

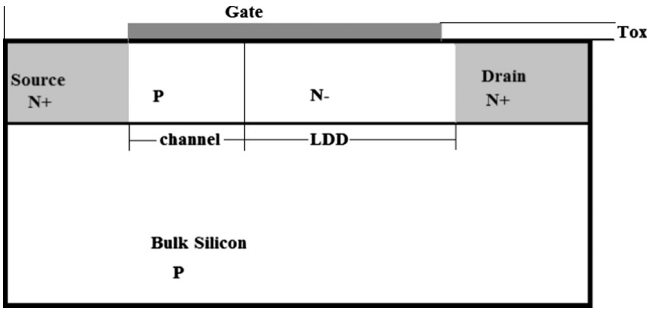

Fig. 1. Structure of a NLDMOSFET.

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