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Negative differential resistance in porous silicon devices at room temperature

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ABSTRACT

We report a voltage controlled negative differential resistance (NDR) effect at room temperature in two types of devices based on porous silicon (PS): thermally oxidized porous silicon multilayer with Ag electrodes in a sandwich configuration (Ag/c-Si/PS/Ag) and porous silicon single layer with Al electrodes in a coplanar configuration (Al/PS/Al). The NDR effect was observed in current–voltage characteristics and showed telegraphic noise. The NDR effects showed a strong dependence with temperature and with the surrounding atmospheric air pressure. The NDR occurrence was attributed to the blocking of conduction channels due to carrier trapping phenomena. We also experimentally demonstrate porous silicon devices exploiting the NDR effect, with potential applications as volatile memory devices.

1. Introduction

Porous silicon (PS) has been one of the most studied materials in recent years [1,2]; however, many of its properties do not have satisfactory explanation, remaining matter of debate. Among its

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interesting properties are quasibalistic electronic emission [3], electric-field induced switching of diode polarity [4], photoluminescence in the visible [5] and tunable optical properties [6]. In addition, due to its low cost of production and versatility, PS provides a wide range of technological applications.

The negative differential resistance (NDR) is a phenomenon of technological interest due to its multiple applications in electronics, such as in memory devices, oscillators and fast switching devices [7]. This effect was first observed in Esaki diodes [8] and in recent years it has been demonstrated in several semiconductor systems, including organic semiconductors [9], molecular nanowire junctions [10] and single electron devices [11]. Regarding silicon based devices, NDR has been observed also in amorphous silicon/silicon carbide devices [12], Si/SiO_2 nanowire, or quantum dot based devices [13] and also in porous silicon [14,15].

The NDR effect is not associated with a single physical mechanism. A large variety of phenomena, such as tunneling [7], Coulomb blockade [13], charge storage [16], and other effects have been suggested as causes for the NDR. In this work, we discuss the NDR behavior observed in two different kinds of PS devices: (1) vertical, thermally-oxidized, PS multilayer structure, which has been reported as an efficient electron emitter [3], and (2) planar, single layer PS devices, which are being investigated as promising gas-sensors. Interestingly, both types of devices present very similar transport characteristics when brought into the NDR state, which we attribute to a common dominant mechanism controlled by Coulomb repulsion effects.

We also propose a simple device that integrates PS structures to demonstrate the potential applications of their NDR phenomena in volatile memory devices.

2. Materials and methods

All the PS-based devices studied in this paper (multilayer PS devices and single layer PS device) were prepared by electrochemical anodization of crystalline p-Si (ρ = 2–4 mΩ cm) with ⟨100⟩ orientation.

In order to obtain PS multilayers with Ag electrodes in sandwich configuration, the crystalline silicon wafers were anodized in a 1:2 solution of HF (50%):Ethanol alternating high (60 mA/cm^2) and a low (20 mA/cm^2) current densities. This procedure resulted in alternate layers having two different porosities [6]. The etching process was designed to obtain structures with 8 layers of each porosity. As a result of the anodization process with high current densities layers with a porosity of 78% and a thickness of 86.1 nm were obtained, while for low current densities layers with a porosity of 60% and a thickness of 69.5 nm were obtained, so the total thickness of the multilayer samples was 1.25 μm. The top contact (Ag/SP) was deposited on the PS multilayer samples by electroless technique using a silver nitrate solution. The bottom contact (Ag/c-Si) was made with conductive silver paint. Finally, the devices were annealed at 300 °C for 5 min in air, a procedure that results in the formation of a 2–4 nm thick surface silicon oxide layer [17]. We will name these structures in the text as Ag/c-Si/PS/Ag.

PS layers with Al electrodes in a co-planar configuration were also studied. These samples were fabricated by anodizing crystalline silicon wafers in a 1:2 solution of HF (50%):Ethanol with a current density of 20 mA/cm^2. The resulting films are mesoporous (pore size of 5–10 nm) with porosity of 60% [4]. The anodization times were 200 s in order to obtain PS films with thicknesses of 2 μm. The PS films were separated from the silicon substrate by anodization in a 1:7 HF (50%):Ethanol solution using a short pulse of high current density (360 mA/cm^2). These PS layers were then transferred to glass slides previously coated with two aluminium contacts separated by a gap of 20 μm. The transferred layers were dried under N_2 flow, forming mechanical Al/PS contacts. We will name these structures in the text as Al/PS/Al.

I–V experiments for Ag/c-Si/PS/Ag sandwich devices were made at atmospheric pressure and room temperature. Experiments with Al/PS/Al planar devices were made at 5×10^{-6} Torr, at different temperatures.

For detection of quasi-ballistic electrons, a metallic plate was placed at 10 mm from the sample surface. The device was placed into a vacuum chamber (1×10^{-5} Torr) and was biased between