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Low specific on-resistance power MOSFET with a surface improved super-junction layer

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A novel low specific on-resistance ($R_{on,sp}$) integrable power metal-oxide-semiconductor field-effect transistor (MOSFET) with a surface improved super-junction (SISJ) layer is proposed. A super-junction layer is implemented at the surface of the drift region and the P pillar in super-junction layer is split into two parts with different doping concentrations. Firstly, the super-junction layer causes the multiple-direction depletion effect. The drift region doping concentration of the SISJ LDMOS is therefore increased significantly. Secondly, the super-junction layer provides a surface low on-resistance path. Thirdly, the new electric field peak introduced by the variation in the doping concentration of the P pillar modulates the surface electric field distribution, resulting in an improved breakdown voltage (BV). It reduces the device pitch for a specific BV capacity. All of them decrease $R_{on,sp}$ sharply. The SISJ LDMOS exhibits a $R_{on,sp}$ of 10.2 mΩ cm^2 for BV = 230 V and decreases $R_{on,sp}$ by 37% compared with a conventional lateral double-diffused MOSFET (LDMOS) at the same BV. Finally, because of the shallow depth of the SISJ layer, the proposed structure can be compatible with CMOS technology. Consequently, the SISJ LDMOS must be a competitive power device for power integrated circuit applications.

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1. Introduction

Lateral double-diffusion MOSFET (LDMOS) acts as an important component in power electronics applications for its facility integration. The desired performance of LDMOS is the use of the lowest specific on-resistance ($R_{on,sp}$) to decrease conduction loss at a certain breakdown voltage (BV). Some new structures have been reported [1–4]. Super-junction (SJ) concept [5,6] used in LDMOS [7] further improves the trade-off between the BV and $R_{on,sp}$. Based on a SJ concept, several new structures have been developed [8–13]. In particular, with the development of smart power integrated circuit (SPIC), it is very crucial to design an LDMOS integrated in SPICs implementing in a CMOS-compatible process [14].

In this letter, we propose a novel LDMOS with a surface improved super-junction (SISJ) layer. The SISJ layer not only increases the doping concentration of the drift region but also provides a surface low on-resistance path. And the new electric field peaks caused by the SISJ layer modulates the surface electric field distribution, leading to an improved BV. The device pitch is therefore reduced for a specific BV. As a result, the SISJ layer decreases the $R_{on,sp}$ steeply. In addition, this device structure is compatible with CMOS technology which can be facilely integrated in SPICs.

2. Device structure and mechanism

The proposed SISJ LDMOS and its physical mechanism are illustrated in Fig. 1. A SJ layer is located at the surface of the drift region and the P pillar is split into two parts with doping concentrations N_p

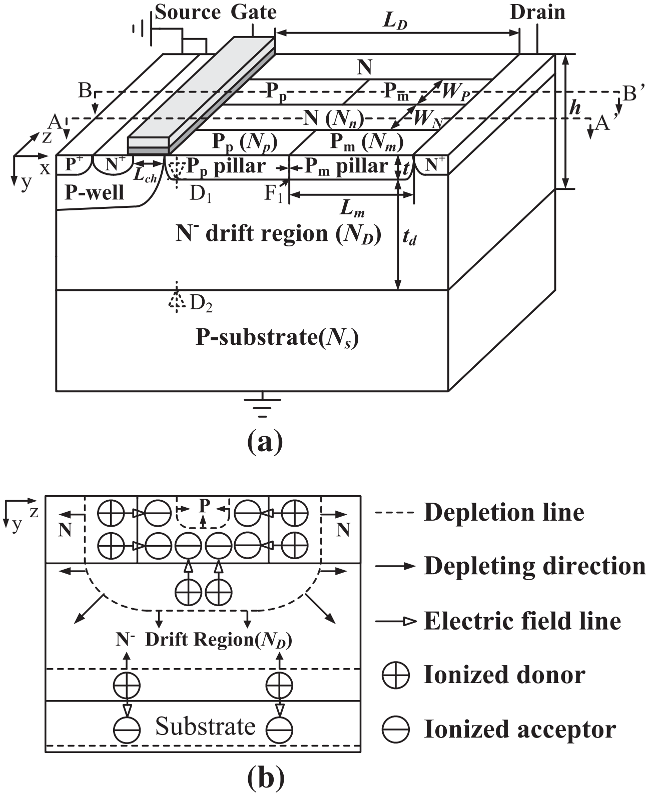

Fig. 1. (a) The structure of the SISJ LDMOS. (b) Schematic diagram for charge balance.