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A novel SOI MESFET by reducing the electric field crowding for high voltage applications

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ABSTRACT

In this paper, a novel silicon-on-insulator (SOI) metal–semiconductor field-effect transistor (MESFET) is presented by reducing the electric field crowding. The charge distribution in channel modifies by reducing the electric field crowding and results in the breakdown voltage (V_{BR}) improves. To reduce the electric field crowding, a buried field plate (BFP) is employed in the buried oxide of the SOI MESFET and connected to source. DC and frequency response characteristics of the SOI MESFET with BFP (BFP-SOI MESFET) are analyzed via a 2-D numerical simulation and the results are compared with characteristics of a conventional SOI MESFET (C-SOI MESFET) structure. The BFP has outstanding effect on the V_{BR} of the device. The V_{BR} of the proposed BFP-SOI MESFET improves by 84% compared with that of the C-SOI MESFET. Although the saturation drain current of the proposed structure has decreased to a small extent, 37% increase in maximum power density is obtained. In addition, the proposed structure showed an approximately 70% decrease in the gate-drain capacitance (C_{gd}), which in-turn resulted in 5 dB maximum available gain (MAG) improvement at 2 GHz. As a result of employing the buried field plate, the BFP SOI-MESFET has an outstanding DC and frequency response performance compared with the C-SOI MESFET.

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1. Introduction

Today, silicon-on-insulator (SOI) technology has demonstrated its potentialities for high frequency and low-power-consumption applications such as use in harsh environments and various commercial applications. SOI also offers high resistive substrate capabilities, leading to substantially reduced substrate loss as well as junction capacitance [1]. Furthermore, metal–semiconductor field-effect transistor (MESFET) is an outstanding contender of MOSFET in VLSI/ULSItechnology [2–4] due to the following features: enhanced radiation hardness [5], immunity to hot carrier aging [6], scaling well [7], and less mobility degradation [8]. SOI MESFETs have drawn considerable attention for their high-power and high-speed applications. In addition, SOI MESFETs have been well-matched to mainstream CMOS processing. Although SOI MOSFETs are more investigated and studied, the SOI MESFET can be an appropriate alternative. Higher mobility of the carriers in the channel region is the main merit of SOI MESFET in contrast with that of the SOI MOSFET. Since the depletion region of schottky gate in SOI MESFET structure conducts carriers into the bulk. In turn, it leads to their increase of mobility to that of the bulk material. So higher intrinsictransconductance (g_m), current and frequency features can be achieved [9]. In addition, the absence of gate-oxide connection in the SOI MESFET structure enables device to tolerate high voltages. The breakdown voltage (V_{BR}) is also at least three times greater than that of the SOI MOSFET structure [9–11].

On the other hand, the upside of such structures makes them immune to problems raised from oxide–semiconductor interface which almost all SOI MOSFETs encounter such as interface traps and reliability issues arising from hot electron injection and trapping [12]. Additionally, the schottky metal gate allows for an enhanced control on the channel region which is significant for high-speed applications. Consequently, the SOI MESFET structure can be taken into account as a device with outstanding frequency response and can be utilized for RF high power applications. Due to advantages of the SOI MESFET characteristic enhancement, several investigations for the SOI MESFET structure have been reported [13–18]. The modification of charge distribution has a considerable influence on device characteristics [19–23].

This paper introduces a novel SOI MESFET structure to improve the device performance. The main idea of this work is to modulate the charge distribution of channel region with the aim of decreasing the electrical field crowding of device and enhancing the V_{BR}. A field plate is placed in the buried oxide (BOX) and connected to source for modifying the charge distribution. Therefore, we called the proposed structure as the buried field plate (BFP) SOI MESFET. The characteristics of proposed structure such as hole concentration, electric field distribution, V_{BR}, potential distribution, drain current (I_D), output power density, unilateral power gain (U), maximum available gain (MAG), and current gain (h_{21}) are investigated by a numerical simulation. The results demonstrate the BFP SOI-MESFET has superior DC and frequency response performances compared with a conventional SOI (C-SOI) MESFET.

2. BFP-MESFET structure and simulation method

The cross section of C-SOI MESFET and BFP-SOI MESFET structures are shown in Fig. 1. The proposed structure is stacked by p-type substrate, a BOX, an n-type channel layer, and two highly doped n-type cap layers. Compared with the C-SOI MESFET structure, there is an added field plate that is connected to the source terminal and stretches out under the gate to the gate-drain region in the BOX of the proposed structure. The dimensions of the BFP-SOI MESFET are as follows: The source and drain lengths are identical and equal to 0.5 μm, gate length L_G = 0.6 μm, gate-drain spacing, L_{GD} = 0.6 μm, and gate-source spacing is L_{GS} = 0.6 μm. The p-type substrate layer thickness is also 0.1 μm with doping of 1×10^{13} cm^{-3}, the BOX thickness is 0.4 μm, the n-type active layer is doped at 1×10^{17} cm^{-3} with a thickness of 0.2 μm, and the n-type cap layers have doping level >10^{20} cm^{-3}. Nickel is selected for the gate Schottky contact with a work function (ϕ_m) of 5.1 eV. L and H are the length and height of BFP, respectively. D is the distance between the BFP and the BOX surface. After optimization of the BFP location, L = 2 μm, H = 0.05 μm, and D = 0.05 μm are achieved. By default, a temperature of 300 K is utilized in the numerical simulations. The C-SOI MESFET parameters are analogous with those of the BFP-SOI MESFET with one exception; the C-SOI MESFET does not have the BFP.