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A 700 V narrow channel nJFET with low pinch-off voltage and suppressed drain-induced barrier lowering effect ☆

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ABSTRACT

This paper proposes a 700 V narrow channel region triple-RESURF (reduced surface field) n-type junction field-effect transistor (NCT-nJFET). Compared to traditional structures, low pinch-off voltage (V_P) with unobvious drain-induced barrier lowering (DIBL) effect and large saturated current (I_{Dsat}) are achieved. This is because p-type buried layer (Pbury) and PWELL are introduced to shape narrow n-type channel in JFET channel region. DIBL sensitivity (S_{DIBL}) is firstly introduced in this paper to analyze the DIBL effect of high-voltage long-channel JFET. Ultra-high breakdown voltage is obtained by triple RESURF technology. Experimental results show that proposed NCT-nJFET achieves 24-V V_P, 3.5% S_{DIBL}, 2.3-mA I_{Dsat}, 800-V OFF-state breakdown voltage (OFF-BV) and 650-V ON-state breakdown voltage when V_{GS} equals 0 V (ON-BV).

1. Introduction

In order to start up or power up the IC, high voltage (HV) JFET is widely used in AC–DC converter and LED driver [1–8]. As is shown in Fig. 1, when IC starts up JFET is turned on to supply the

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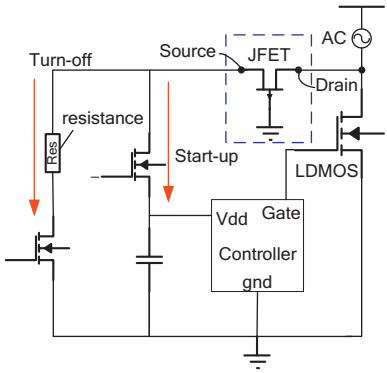

Fig. 1. Typical application circuits for HV-JFET.

consumption of internal circuits. To realize high response rate of loops, the JFET should have large I_{Dsat} [9]. After IC starts up, the JFET is turned off by the increasing source-gate voltage V_{SG} with a large current-limiting resistance connected to the source electrode. The pinch-off voltage (V_P) is thus defined as the turn-off voltage V_{SG} of the JFET and a low and steady V_P is required in the circuit to reduce the burden of the inner controller. Unfortunately, DIBL effect in HV JFET will make the V_P shift with increase of V_{DS} and influence the operative stability. 700 V double RESURF nJFETs (DO-nJFET) combined with double RESURF nLDMOS are proposed in Refs. [10,11]. Compared with independent JFET, this composite structure saves more layout area and avoids the difficulty of HV interconnection. Another single buried layer nJFET (SB-nJFET) which has larger I_{Dsat} due to triple RESURF technology is proposed in Ref. [12]. However, without p-type layer in JFET channel region, V_P and DIBL effect are both large. A super-junction nJFET proposed in Ref. [13] achieves low V_P with low DIBL effect, which leads to high process cost because of the SOI material and super junction technology.

This paper proposes a 700 V NCT-nJFET which is fully compatible with the 700 V BCD process platform. n-Type channel region is depleted by the second Pburied layer and PWELL layer. Therefore narrow channel is achieved which is benefit for the low V_p and small DIBL effect. Compared with traditional HV JFETs, this new structure features an adjustable low pinch-off voltage with unobvious DIBL effect, high voltage block capability and large saturation current.

2. Device structure and mechanism

Fig. 2(a) shows the top view of NCT-nJFET which shares common drain electrode with triple RESURF nLDMOS (T-nLDMOS). Gate electrode is shorted to ground by PWELL layer which means V_{SG} equals V_S. High breakdown voltage is obtained by long n-type drift region NWELL. Channel region is a high-resistance region which can not only prevents large current flowing past the device to increase ON-BV, but also supplies a low and adjustable pinch-off voltage by varying channel width W_2. Pburied1 is introduced in drift region to keep charge balance with NWELL. Pburied2 overlying PWELL decreases the thickness of conducting layer to help channel region deplete. Then low V_P with unobvious DIBL effect is achieved. Pburied1 and Pburied2 are both shaped by the same mask layer Pbury. Fig. 2(b) shows the cross-sectional view of NCT-nJFET along line AA′. Pburied2 are absent or replaced by PTOP layer for SB-nJFET and DO-nJFET in Fig. 2(c) and (d), respectively. With the same thicknesses of NWELL and p-type layers, H_2 of NCT-nJFET is less than that of the other two structures, which makes channel easier to be pinched off for NCT-nJFET. Manufacturing process of proposed NCT-nJFET is shown in Fig. 3. Without any other special steps, it can be easily integrated in bulk-silicon 700 V BCD process using triple RESURF technology.