Superlattices and Microstructures 55 (2013) 131–143

Contents lists available at SciVerse ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Gold Schottky contacts on (002) CdSe films growing on p-type silicon wafer

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ARTICLE INFO

Article history:
Received 7 November 2012
Accepted 10 November 2012
Available online 5 December 2012

Keywords:
CdSe
II–VI Semiconductors
Semiconductor devices
Heterostructures
Schottky contacts
Inhomogeneous barrier height
Space charge limited current

ABSTRACT

The thermal evaporation technique has been successfully used for depositing CdSe on p-Si (001) substrates. X-ray diffraction analysis indicated the hexagonal structure for the growing film along the (002) plane with *c*-axis perpendicular to Si-substrates. The average particle size was calculated to be ~40 nm with a dislocation density at the film surface of 6.25×10^{10} cm^{-2}. The temperature dependent electrical properties of Au Schottky contacts to *a*-plane CdSe thin films growing on p-Si (001) were investigated over the temperature range of 160–360 K, which show a rectification behavior. The barrier height (φ_b), and ideality factor (n), values were found to be 0.863 eV at 360 K to 0.451 eV at 160 K, and 2.48 ± 0.11 at 360 K to 5.18 ± 0.19 at 160 K, respectively. The increasing of φ_b while decreasing n with the increase of temperature was described by a double Gaussian distribution with two different regions in the temperature range of 240–360 and 160–240 K. Moreover, it was observed that Au/CdSe/Si/Al heterostructure exhibit space charge limited current (SCLC) at all temperatures. The transition voltage (V_x) from ohmic to SCLC is found to be quite dependent on temperature. The defect levels were estimated from the slope of ln$J$ versus $1/T$ plots, which yield two values of activation energies $\Delta E_{d1} = 0.227 \pm 0.011$ eV in the 240–360 K range and $\Delta E_{d2} = 0.128 \pm 0.003$ eV in the 160–240 K range, respectively.

1. Introduction

Among the II–VI compound semiconductors, cadmium selenide (CdSe), with a direct band gap of 1.74 eV at room-temperature (RT), has gained a great deal of attention for its potential applications

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http://dx.doi.org/10.1016/j.spmi.2012.11.013

in the fields of light amplification, gamma-detectors [1], thin film transistors [2], solar cells [3], and acousto-optic devices [4]. Different deposition techniques have been carried out to prepare CdSe; these include: chemical deposition, vacuum evaporation, molecular beam epitaxy, metal oxide molecular beam epitaxy, and Laser ablation (*c.f.* [5,6] and references cited therein). Here, the quality of a device strongly depends on both structure and electronic properties of the CdSe films which, in turn, depends on the experimental conditions [7]. In order to achieve high performance CdSe devices, it is essential to develop reliable and reproducible Ohmic and Schottky contacts. Along with Schottky barriers, ohmic contacts represent the two basic metallization technologies for semiconductor device fabrication. Ideally, a metal-semiconductor (MS), junction results in an ohmic behavior if the barrier formed by the contact is zero. In both cases, however, it is necessary for the electrical contacts to be steady with time and to operate at various temperatures and in various ambient without degradation. Nevertheless, many cases have significant deviations from the ideal Schottky barrier contacts behavior; i.e., increase in ideality factor and decrease in barrier height with temperature decrease. All specified deviations are known for some decades; however, their nature is still a subject for discussion up to date [8]. In fact, the interfacial states of the MS contacts have a dominant influence on the device performance, reliability and stability [8,9] as well as the current across the MS contact that may be greatly influenced by the presence of barrier height inhomogeneities. It is therefore necessary to understand the electrical properties of such diodes, in particular, the current–voltage (I–V) characteristics and relevant diodes parameters such as ideality factor (n), and barrier height (φ_b).

Nevertheless, a complete description of the charge carrier transport through a MS junction still remains a challenging problem [7,10–14]. An investigation of the I–V characteristics of the MS as well as homo- and heterojunction diodes that measured only at RT does not provide detailed information about the current-conduction process and the formed nature of the interface barrier. There is a barely number of studies that checked up the Au/CdSe configuration viewing spread in φ_b values [13–15], suggesting that the interface structure significantly modifies the electronic environment at the contact.

In the present study, the fabrication of Au/CdSe/p-Si/Al configuration is considered to scrutinize the forward bias I–V characteristics over a temperature range of 160–360 K, aiming to provide some detailed knowledge about the electrical properties, surface morphological evolution and the temperature dependence of Au/CdSe/p-Si/Al heterostructure parameters.

2. Experimental

Thin films of CdSe were deposited from CdSe powder (Balzers, 99·999%) by the thermal evaporation technique using Edwards vacuum coating system (model: E306A) from tungsten boat. The deposition made onto cleaned mirror polished p-Si (0 0 1) wafers at a substrate temperature of 300 K under a vacuum of 10^{-6} Torr. The used substrates were initially cleaned chemically in acetone and isopropyl alcohol ultrasonic bath and then dried using dry nitrogen, followed by a submersion of the Si wafers into an aqueous solution of hydrofluoric acid and hydrogen peroxide with a volume ratio of HF 50%:H_2O_2 30%:H_2O = 1:5:10. This solution etches wafer surfaces to eliminate the native oxide layer at the surface. Aluminum (Al) and gold (Au) electrodes were deposited from tungsten filaments. The deposition rates showed$\sim$2 nm s^{-1} (CdSe), 1 nm s^{-1} (Au), and 1 nm s^{-1} (Al), which continuously monitored using a quartz-crystal monitoring system. Ohmic contact was created at the back side of the wafer by Al (Fluka, 99.999%) electrodes. For the temperature-dependent I–V measurements, the top contact is prepared by evaporating chemically pure Au (Loba, 99.99%) with a thickness of $\sim$250 nm and diameter of 5 mm over a contact area of 0.196 cm^2. The obtained film was found to have a thickness of 792 nm, as measured by transmission spectra in the far-infrared region. After fabrication, the samples were removed to a subsidiary vacuum system maintained at RT under a pressure below 10^{-3} Torr.

The chemical composition as well as the homogeneity of the deposited semiconductor films were checked at several positions using a virtual standard analysis package on a scanning electron microscope (SEM), model: JEOL-5400, equipped with an energy dispersive analysis of X-rays (EDAX) unit comprising a Si(Li) detector. The quantification analysis was calibrated with highly pure constituent elements as standard.