Superlattices and Microstructures 52 (2012) 552–559

Contents lists available at SciVerse ScienceDirect

Superlattices and Microstructures

journal homepage: www.elsevier.com/locate/superlattices

Novel partially depleted SOI MOSFET for suppression floating-body effect: An embedded JFET structure

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ARTICLE INFO

Article history:
Received 13 April 2012
Accepted 6 June 2012
Available online 15 June 2012

Keywords:
Silicon-on-insulator
Floating-body effect
SiGe
Simulation

ABSTRACT

Silicon-on-insulator (SOI) devices have an inherent floating body effect which may cause substantial influences in the performance of SOI devices and circuits. In this paper we propose a novel device structure to suppress the floating body effect by using an embedded junction field effect transistor (JFET). The key idea in this work is to provide a path for accumulated holes to flow out of the body to improving of electrical performance. We have introduced a p^+-$Si_{1-x}Ge_x$ buried region under the n^+-$Si_{1-x}Ge_x$ source and called the proposed structure as embedded JFET SOI MOSFET (EJFET–SOI). Using two-dimensional two-carrier simulation, the output and subthreshold characteristics of EJFET–SOI are compared with those of conventional SOI counterparts. The simulated results show the suppression of floating body effect in the EJFET–SOI structure as expected without consuming a significant amount of area.

1. Introduction

Silicon on insulator (SOI) technology exhibits many advantages over bulk silicon technology such as the reduction of parasitic capacitances, excellent subthreshold slope, elimination of latch up, and resistance of radiation. It is widely used in realm of high-speed, high-temperature and low-power circuits. Partially depleted (PD) SOI devices are preferred to fully depleted (FD) ones, because the threshold voltage in PD SOI device is less sensitive to the uniformity in the silicon film thickness [1]. However, in a partially depleted (PD) SOI MOSFET, the bottom portion of the silicon film under the channel region is electrically floating. Hence, the floating body effect becomes an inherent issue in a PD SOI MOSFET [2]. This effect causes lowering of the drain breakdown voltage, kink effect [1],

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http://dx.doi.org/10.1016/j.spmi.2012.06.006

abnormal sub-threshold slope and current instability in switching operation, and so on. These phenomena are caused by the isolation of the channel region from the substrate by the buried oxide layer and the accumulation of holes generated by the impact ionization near the drain region.

There are two approaches to mitigate the floating body effect. One is to provide body contacts, but this method suffers from an area penalty. Moreover, the efficiency of hole absorption decreases rapidly as the channel width increases. The other approach is to use source engineering techniques that are independent of the channel width [1,3]. These techniques include the formation of recombination centers at the source/drain junction by using argon ion implantation, bipolar embedded source structure formation by Si^+ implantation, and bandgap narrowing of the source region utilizing Ge ion implantation [4–6]. However, this technique should not effectively mitigate the floating body effects in a p-MOSFET and drain breakdown voltage might deteriorate with an increase of Ge content.

The challenge that we have addressed in this paper, therefore, is to examine if we can provide a path for accumulated holes to flow out of the body by introducing an embedded junction field effect transistor (JFET), this should result in a high performance MOSFFET.

Based on the above idea, the aim of this paper is therefore to propose for the first time, a new device structure called the Embedded JFET SOI MOSFET (EJFET–SOI) in that a p^+-$Si_{1-x}Ge_x$ buried region is introduced under the n^+-$Si_{1-x}Ge_x$ source. Numerical simulations are carried out with a two-dimensional device simulation program ATLAS [7] to predict electrical characteristics, and the output characteristics and gate characteristics are compared with the conventional SOI MOSFET (C-SOI). The potential contours and hole current vector are also simulated to elucidate the suppression mechanism. Our results suggest that the embedded JEFET in the proposed structure expedites the dispersion of holes generated by impact ionization and it is believed that they are primarily responsible for the mitigation of the floating body effect.

2. Device design and simulation

Fig. 1 shows the cross-section of the simulated n-channel EJFET–SOI structure. As can be seen from the figure, a p^+-$Si_{1-x}Ge_x$ buried region is introduced under the n^+-$Si_{1-x}Ge_x$ source for creating an embedded pJFET in the proposed structure. Also, the p^+-$Si_{1-x}Ge_x$ buried region is extended to the channel region. It is noticed that the n^+ source of the MOSFET acts as the gate of the pJFET and the p^+ region underneath the n^+ source acts as the channel of the JFET. This embedded JFET connects the body and source (as shown at the schematic in Fig. 2), and the underlying p^+ region (the channel of the JFET) provides a low-barrier path for the holes generated by impact ionization. The end result is that the $Si_{1-x}Ge_x$ source and buried p^+ region will both increase the hole current to the source. The details of the relevant parameters are given in Table 1. As compared with the proposed structure, we also simulate a conventional SOI MOSFET (C-SOI). Its parameters are the same as the former,

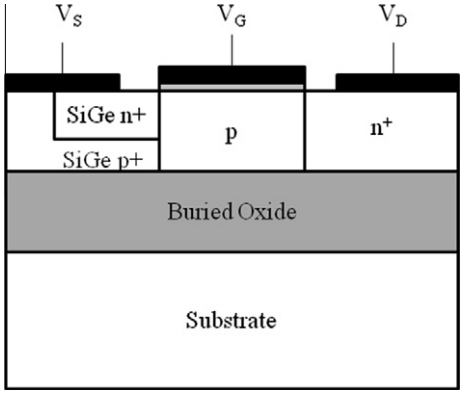

Fig. 1. Cross section of the novel EJFET–SOI.