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Breakdown voltage improvement of LDMOSs by charge balancing: An inserted P-layer in trench oxide (IPT-LDMOS)

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ABSTRACT

For the first time, the novel inserted P-layer in trench oxide of LDMOS structure (IPT-LDMOS) is proposed in which a trench oxide with inserted P-layer is considered in the drift region to improve the breakdown voltage. Our simulation with two dimensional ALTAS simulator shows that by determining the optimum doping concentration of the P-layer, the charges of the N-drift and P-layer regions would be balanced. Therefore, complete depletion at the breakdown voltage in the drift region happens. Also, electric field in the IPT-LDMOS is modified by producing additional peaks which decrease the common peaks near the drain and source junctions.

1. Introduction

High performance power transistor is essential for integrated circuits and discrete power devices. Among different power transistors, Lateral Double Diffused MOSFET (LDMOS) structure has been widely used in intelligent power applications [1–3]. In another vision, silicon on insulator (SOI) technology has been attracted much attention in power ICs due to the low leakage current, higher switching speed, considerable reduction in parasitic capacitance and so on [4]. However, low vertical breakdown voltage in SOI devices is the major problem that restricts power applications. In order to increase breakdown voltage in such devices, many novel structures have been proposed in which modifying the electric field distribution in the drift region is the effective solution [5–7].

Another challenge in the power device design is obtaining small specific on-resistance [8,9]. Two significant methods which reduce specific on-resistance are obtained by a high doping concentration in drift region and short drift length [10]. But, these solutions reduce breakdown voltage [9–11]. In order

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to achieve the best characteristic of LDMOS in both of breakdown voltage and specific on-resistance, a novel structure has been proposed in this paper. The goal of the present work is incorporating trench oxide with inserted P-layer in the drift region. The proposed structure which is named as inserted P-layer in trench oxide of LDMOS (IPT-LDMOS), exhibits the best characteristics in terms of breakdown voltage and specificon-resistance.

An interesting mechanism occurs to improve breakdown voltage of IPT-LDMOS. The inserted P-layer helps reducing the surface electric field and simultaneously increases the breakdown voltage. It means that when the device switches in the OFF state with high drain voltage, the depletion width of the reverse-biased junction between the inserted P-layer and N-drift will increase. So, it helps to deplete the drift region and also increase the breakdown voltage. It is important to note that when the transistor is in the ON state with a low drain voltage, the depletion width of the reverse-biased junction is small which have a few influences on the ON-state current. Also, the P-layer is doped to achieve a balanced charge condition which means that the charge of depletion layer is zero.

Our simulation with two dimensional ATLAS simulator shows the P-layer in the trench oxide helps to reduce the drift length without further decreasing the conduction area [12]. So, the specific on-resistance of the IPT-LDMOS is reduced effectively as compared with Conventional LDMOS structure (C-LDMOS) which the trench oxide and the P-layer are not considered in the drift region.

2. Device structure and simulation

The schematic cross section of the IPT-LDMOS is illustrated in Fig. 1. As the figure shows the trench oxide is located in the drift region and a P-layer is inserted in it with the length of L_P and the depth of D_P. Also, the length and depth of trench oxide are labeled as, L_T and D_T, respectively. The thicknesses of buried oxide and silicon layer are 0.3 and 0.6 μm, respectively. The length and depth of P-layer as well as its doping concentration is determined in the next part. The IPT-LDMOS parameters used in our simulation are shown in Table 1. All the device parameters of the new structure are equivalent to those of the C-LDMOS unless otherwise state.

Two dimensional numerical simulations of the proposed structure are done with ATLAS simulator. In addition to, Poisson and drift/diffusion equations, SRH (Shockley-Read-Hall) and Auger models are considered for generation/recombination, and also IMPACT SELB for impact ionization. These simulations methods allow taking into account carrier velocity saturation, carrier–carrier scattering in the high doping concentration, dependence of mobility on temperature and vertical electric influence [13].

It is worth noting that the two dimensional (2D) simulator is calibrated to experimental data [14]. The transfer characteristics at the drain bias of 0.1 V of SOI-LDMOS, is extracted from experimentally measured have been compared with ATLAS simulation in Fig. 2 [14]. It can be seen from the figure that a good agreement between experimental data and 2D simulation results is achieved.

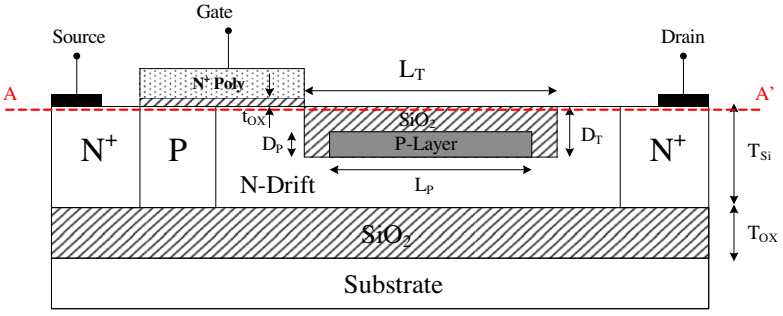

Fig. 1. Schematic of Inserted P-layer in trench oxide of LDMOS (IPT-LDMOS).