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Simulation and optimization of high breakdown double-recessed 4H-SiC MESFET with metal plate termination technique

Hossein Elahipanah *

Islamic Azad University, Mahdishahr Branch, Semnan, Iran

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In this paper a new high breakdown voltage (V_{BR}) double-recessed 4H-SiC MESFET with metal plate (DRMP-MESFET) structure for reliable high power and RF applications is proposed. The maximum electrical field of the MESFET gate is clamped after surface depletion layer punch through to the metal plate (MP). The influence of MP structure on the breakdown voltage and cut-off frequencies of the DRMP-MESFET was studied by numerical device modeling. The optimized results showed that the V_{BR} of the proposed structure with metal plate is 95% and 55% larger than that of the 4H-SiC double-recessed MESFET without metal plate (DR-MESFET) and conventional recessed-gate MESFET (R-MESFET), respectively, while maintaining almost the same saturation drain current characteristics. A maximum 12.6 W/mm output power density of the proposed structure with metal plate is reached compared to 6.1 W/mm and 4.4 W/mm for the DR-MESFET and R-MESFET, respectively, which means about 107% and 186% larger output power. Also, cut-off frequencies (f_T) of 14.7 GHz and 16.2 GHz and maximum oscillation frequencies (f_{max}) of 54.3 GHz and 64.1 GHz for the 4H-SiC DRMP-MESFET and DR-MESFET are obtained compared to 11 GHz and 40 GHz for that of the R-MESFET structure, respectively. The simulation results reveal that a 95% improvement in V_{BR} can be obtained with a metal plate while not significantly reducing its cut-off frequency.

* Tel.: +98 2313343431; fax: +98 2313343431.
E-mail address: elahipanah@ieee.org.

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1. Introduction

Silicon carbide (SiC) MESFETs offer significant advantages for high voltage, high power and high temperature applications due to their superior properties and the relatively mature device fabrication technology, such as wide band gap (3.26 eV), high breakdown field (3 MV/cm), large thermal conductivity (4.5 W/cm K) and high electron saturation velocity (2×10^7 cm/s) [1,2]. The increased power density and higher operating voltage enable higher performance, lighter weight, and wider bandwidth systems compared to those using conventional technologies based on Si and GaAs [1–3]. With the recent progress in SiC epitaxial material and device processing, impressive performances for SiC MESFETs have been reported [4,5]. Among its polytypes, 4H-SiC has gained much attention as its electron mobility is about twice as high as that of 6H-SiC. 4H-SiC MESFETs used for power applications must be able to sustain a large drain current as well as have high electric fields. To allow for high drain current, a large product of the channel doping and thickness ($N \times t_C$) is required. However, a higher channel doping concentration will lower the breakdown voltage (V_{BR}) [6], and a thick channel layer will lead to a lower aspect ratio of gate length to channel thickness (L_G/t_C) and result in a drain-induced barrier lowering (DIBL) effect which will degrade the device and circuit performance [6]. In order to overcome this challenge, structures such as split gate [7] and double-recessed 4H-SiC MESFET (DR-MESFET) [8] are proposed to allow a thicker channel while maintaining a larger L_G/t_C. Therefore, the DR-MESFET structure has lower and upper gates, which control a thinner and a thicker part of the channel, respectively. The thicker channel allows for a higher drain saturation current and lower source and drain impedances, whereas the thinner channel ensures that the channel can be effectively controlled by the gate bias.

Although the experimental and simulation results in previously published literature have shown that 4H-SiC MESFETs have higher breakdown characteristics compared to those made with Si and GaAs [9–12], it is still worth investigating potential ways to increase the breakdown voltage to better meet the increasing demand for high power and RF applications. The 4H-SiC DR-MESFET has better performance compared to similar devices based on the conventional recessed-gate (R-MESFET) structure. However, with the increase of saturation drain current, the device performance is degraded in the form of a decreased breakdown voltage due to the larger channel thickness between gate and drain [8]. Therefore, to reach the superior characteristic of the DR-MESFET structure, it is necessary to find a solution to this problem. Much research on 4H-SiC devices has shown that the breakdown happened at the gate corner nearer to the drain side on the device surface due to electric field crowding, which can become large near breakdown and creates potential reliability concerns [12–16]. In order to suppress the peak electric field as well as alleviate the electric field crowding in the drain side gate corner, recently specialized edge termination structures have been adapted from Si for a variety of SiC devices in order to suppress electric field crowding at the device periphery, and can generally be categorized as techniques, or a combination of techniques, involving field plates, floating guard rings, junction termination extensions (JTE), or junction beveling (mesas) [17–24]. Termination structures were examined with respect to device type, the influence of oxide charge, and current processing limitations.

Metal ring termination is a widely used termination method in Si technology, which has recently been employed in SiC devices [22–25]. In metal ring structures, junction shielding is accomplished by a ring that becomes biased when the encroaching depletion region contacts each junction. The potential of the ring will then follow the potential of the main junction within the punch through value. This has the effect of distributing the high edge field of the main junction to the edge of the biased ring. In this paper, we employ a similar mechanism to inhibit avalanche breakdown [26,27]. An uncontacted gate element (metal plate), which floats in potential in a manner similar to metal rings, is inserted between the gate and the drain. This decouples the usual inverse dependence of V_{BR} on carrier concentration by clamping the maximum electric field at the main gate to a value less than the avalanche field. The drain voltage is spread over the metal plate and gate, leading to an increased breakdown voltage. Recently, a high-breakdown voltage 4H-SiC MESFET with floating metal strips has been reported [27] based on this technique. One should note that by using this technique, some harmful effects in device performances could appear. By comparing conventional MESFET structures with different lengths, it can be seen that the device characteristics improved when the device length and gate-drain spacing