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Effect of the Ge mole fraction on the formation of a conduction path in cylindrical strained-silicon-on-SiGe MOSFETs

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Abstract

Using two-dimensional simulation, we have demonstrated the effect of the strain or Ge mole fraction x in a $Si_{1-x}Ge_x$ pillar on the conduction path in cylindrical strained-silicon (s-Si) MOSFETs. We show that for low values of the Ge mole fraction x in a $Si_{1-x}Ge_x$ pillar, the conduction path forms in the middle of the cylindrical SiGe pillar and not in the s-Si layer at the surface. Only for large values of the Ge mole fraction x in $Si_{1-x}Ge_x$ pillar does the current conduction path form in the s-Si layer, enabling the advantage of the mobility enhancement of carriers in the device operation. On the basis of our simulation study, we provide the minimum amount of strain or Ge mole fraction x in a $Si_{1-x}Ge_x$ pillar necessary in a device for the current to flow through the s-Si layer.

Keywords: Strained silicon; SiGe; MOSFET; Threshold voltage; Mobility; Two-dimensional simulation

1. Introduction

Scaling down of devices is one of the key methods of enhancing the transistor switching speed. But device length scaling beyond 100 nm has been seriously impeded by the increasing short channel effects (SCEs). Several structures have been proposed for overcoming SCEs, with double-gate (DG) and cylindrical surround gate MOSFETs being the most promising concepts [1–4]. For equivalent silicon and gate oxide thickness, cylindrical MOSFETs can be scaled to 35% shorter channel lengths than DG-MOSFETs for the same SCEs [5]. Cylindrical

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MOSFETs offer additional advantages of improved subthreshold slope, higher packing densities, variable pillar doping (along the channel).

The second main factor controlling transistor switching speed is the carrier velocity (or mobility). Strained Si has been used in recent years to improve carrier transport properties, i.e. mobility and high field velocity, and a number of studies have shown the usefulness of strained silicon in extremely scaled down MOSFETs [6–10].

To incorporate the advantages of both the cylindrical surround gate and the strained silicon, strained-Si surround gate MOSFETs have recently been proposed [11]. This device consists of a SiGe pillar over which silicon is grown so that it becomes strained. The amount of strain created in the silicon layer depends on the Ge mole fraction in the SiGe pillar. In the conventional single-gate or double-gate s-Si MOSFETs, the inversion layer forms (and therefore current flows) near the s-Si/SiO_2 interface of the device. Due to the mobility enhancement in the s-Si layer, these transistors exhibit enhanced drain current. However, we show in this paper that in the case of cylindrical strained-Si-on-SiGe MOSFETs, the inversion layer forms in the center of the SiGe pillar if the Ge mole fraction x in $Si_{1-x}Ge_x$ pillar is not chosen appropriately. To derive the mobility enhancement, the conduction path or the inversion layer must be formed in the strained-silicon layer. Using two-dimensional simulation, we estimate the minimum amount of strain or Ge mole fraction x in the $Si_{1-x}Ge_x$ pillar necessary for the conduction path to be formed in the s-Si layer. We show that the minimum Ge mole fraction x in a $Si_{1-x}Ge_x$ pillar required increases as the pillar diameter increases but is independent of the s-Si layer thickness. An increase in strain or Ge mole fraction x in a $Si_{1-x}Ge_x$ pillar leads to a fall in the threshold voltage of the device [12]. Hence, strain can be introduced effectively in thick-pillar devices only if threshold voltage roll-off can be tolerated.

The simulation work presented in this work is primarily aimed at providing guidelines and motivation for the experimental implementation of cylindrical s-Si-on-SiGe MOSFETs. This study provides the preliminary possibilities and limitations of these devices in order to allow making an appropriate selection of Ge mole fraction x in a $Si_{1-x}Ge_x$ pillar.

2. Strain related models used in 2D simulation

A silicon thin film grown pseudomorphically over a relaxed $Si_{1-x}Ge_x$ substrate experiences biaxial strain leading to changes in band structure [9,13]. Due to strain, the electron affinity of silicon increases and the bandgap decreases. The effect of strain on Si band structure can be modeled as [9,13,14]

$$(\Delta E_C)_{\text{s-Si}} = 0.57x \qquad (\Delta E_g)_{\text{s-Si}} = 0.4x \tag{1}$$

$$\phi_t \ln\left(\frac{N_{V,\text{Si}}}{N_{V,\text{s-Si}}}\right) = \phi_t \ln\left(\frac{m^*_{h,\text{Si}}}{m^*_{h,\text{s-Si}}}\right)^{3/2} \approx 0.075x \tag{2}$$

where x is the Ge mole fraction in the $Si_{1-x}Ge_x$ substrate, $(\Delta E_c)_{\text{s-Si}}$ is the decrease in electron affinity of silicon due to strain, $(\Delta E_g)_{\text{s-Si}}$ is the decrease in bandgap of silicon due to strain, ϕ_t is the thermal voltage, $N_{V,\text{Si}}$ and $N_{V,\text{s-Si}}$ are the densities of states in the valence bands in normal and strained silicon respectively. The energy band parameters for $Si_{1-x}Ge_x$ substrate can also be estimated as [9,13,14]

$$(\Delta E_g)_{\text{SiGe}} = 0.467x, \qquad N_{V,\text{SiGe}} = (0.6x + 1.04(1-x)) \times 10^{19}\ \text{cm}^{-3},$$
$$\varepsilon_{\text{SiGe}} = 11.8 + 4.2x \tag{3}$$