



Modeling of trap-assisted tunneling in AlGa_N/Ga_N heterostructure field effect transistors with different Al mole fractions

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Abstract

Although significant progress has been achieved in GaN based high power/high frequency electronic devices, surface-related problems still need an immediate solution. In particular, leakage currents through Schottky contacts not only impede device reliability but also degrade power efficiency and noise performance in such devices. This article discusses the mechanism of leakage currents through GaN Schottky and AlGa_N/Ga_N Schottky interfaces for both forward and reverse biases. A theoretical model for the calculation of currents based on trap-assisted tunneling is discussed. In the calculation the trap energy has been assumed as a fitting parameter which is about 0.48 eV for different Al mole fractions. The comparison of the results obtained with the existing experimental data in the literature shows a good agreement.

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1. Introduction

AlGa_N/Ga_N heterostructure field effect transistors (HFET) have attracted considerable interest owing to their potential use in high power, high voltage, and high temperature electronic and optoelectronic devices [1,2]. On the other hand the gate leakage current in heterostructure field effect transistors imposes limitations on the device performance, restricting the voltage

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swing and increasing the static dissipation. For years, several research groups have been studying the effect of the gate current in heterostructures FETs with different analytical models that have been proposed. However, most of this study has a lack of accuracy [3]. The purpose of this study is the determining of the gate leakage current in AlGa_n/Ga_n (HFET), including trap levels within the AlGa_n barrier and on the surface between the gate and drain.

2. Theoretical analysis

The band diagram for the AlGa_n/Ga_n heterostructure with the metal contact on top of the AlGa_n barrier has been obtained from self-consistent calculation of Schrödinger and Poisson equations by including all relevant potentials and five subbands within the AlGa_n, and the Ga_n interface well (see Fig. 1).

In the self-consistent calculation, the two-dimensional electron gas density can be obtained from

$$N_s = \frac{\varepsilon(m)}{ed_b} \left(V_G + V_{th}(m) - \frac{\phi_{f_s}(m)}{e} \right)$$

where $\varepsilon(m)$ and d_b are the dielectric constant and thickness for the Al_mGa_{1-m}N barrier, $\phi_{f_s}(m)$ is the Fermi energy with respect to the Ga_n conduction band edge, V_G is the voltage applied to the gate, m is the Al mole fraction in the barrier and V_{th} is the threshold voltage [4].

Knowing the behavior of the 2DEG density as a function of the gate voltage, one can obtain the 2D electron mobility as a function of the gate voltage along the channel [1]. On the other hand, from the charge transport model, the channel potential is well known for AlGa_n/Ga_n heterostructure FETs [5]. Hence the electron temperature can be derived from the energy balance model as [6]

$$T_e(x) = T_0 + \left(\frac{2e}{3K_B} \right) \tau_e(x) \mu_n(x) F(x)^2$$

where x is the distance along the channel starting from the source, $\tau_e(x)$ is the energy relaxation time, K_B is the Boltzmann constant, T_0 is the lattice temperature, $\mu_n(x)$ is the electron mobility and $F(x)$ is the electric field along the 2DEG channel. Knowing all relevant physical quantities from the above calculations, the gate current can be modeled. The gate current, $J_{GT} = J_{sm} + J_{ms}$, is composed of two components: from the semiconductors, AlGa_n and Ga_n, to the metal (J_{sm}) and from the metal to the semiconductors (J_{ms}) [7]. Note that each of the components, J_{sm} and J_{ms} , is further divided into a tunneling component through the barrier, J_T , and a thermally emitted component, over the barrier, J_{TT} .

To calculate the tunneling component, the two-step tunneling via trap, which is called the trap assisted tunneling (TAT) model, has been used [8]. The trap level position within the AlGa_n barrier has been assumed as a fitting parameter of the model with the experimental data and $e\phi_t = 0.45$ eV was achieved (see Fig. 1).

In the gate leakage current study, not only are the deep level traps important but also the surface trap level plays a considerable role, because the ungated surface of the channel between the gate and drain/source of the HFET is a boundary of the active region of the device. These access regions can make a significant contribution to the total source–drain resistance. On the other hand, the gate bias varies the trapping/detrapping of surface states in the ungated region. To calculate these effects and also the surface current due to surface traps, an analytical model has been used [9]. In the model, the lateral tunneling at the drain-side corner of the gate, I_V ,

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