

## Effect of $\text{Bi}_2\text{Ti}_2\text{O}_7$ Seeding Layer on Capacitance-voltage Properties of $\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}$ Films

Huizhong Xu<sup>1,2)</sup>, Liang Zhen<sup>1)†</sup>, Changhong Yang<sup>2)</sup> and Zhuo Wang<sup>2)</sup>

1) School of Materials Science and Engineering, Harbin Institute of Technology, Harbin 150001, China

2) School of Environment and Materials Engineering, Yantai University, Yantai 264005, China

[Manuscript received November 3, 2008, in revised form November 27, 2009]

$\text{Au}/\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}/\text{Bi}_2\text{Ti}_2\text{O}_7/\text{Si}$  structure has been fabricated with a preferentially (111)-orientated  $\text{Bi}_2\text{Ti}_2\text{O}_7$  seeding layer as a ferroelectric gate of metal-ferroelectric-insulator field effect transistor.  $\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}$  and  $\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}/\text{Bi}_2\text{Ti}_2\text{O}_7$  films are both well-crystallized when annealed at  $680^\circ\text{C}$  for 40 min, and have smooth, dense and crack-free surfaces. The width of memory window of the ferroelectric gate increases with increasing electric field applied to the  $\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}$  thin films. The width of memory window of  $\text{Au}/\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}/\text{Bi}_2\text{Ti}_2\text{O}_7/\text{Si}$  with seeding layer is relatively wider than that of  $\text{Au}/\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}/\text{Si}$  at the same bias voltage, and the counterclockwise hysteresis curve of  $\text{Au}/\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}/\text{Bi}_2\text{Ti}_2\text{O}_7/\text{Si}$  is referred to as polarization type switching at different voltages.  $\text{Bi}_2\text{Ti}_2\text{O}_7$  seeding layer plays an important role in alleviating the element interdiffusion between  $\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}$  and Si.

**KEY WORDS:** Metalorganic decomposition; Bismuth titanate; Ferroelectric materials

### 1. Introduction

Ferroelectric devices have attracted attentions for memory applications<sup>[1]</sup>. Among them, the metal-ferroelectric-semiconductor (MFS) has been used as a structure for ferroelectric field effect transistor (FET) type nonvolatile memories. The MFS-FET type is more promising than the ferroelectric random access memory (FeRAM) using a metal-ferroelectric-metal (MFM) structure because the capacitor-type FeRAM is used in a destructive readout mode<sup>[2]</sup>. MFS-FET, in which the spontaneous polarization of ferroelectric films is used as a gate insulator, has the potential advantages, such as high switching speed, nonvolatile data storage, radiation tolerance, and high density<sup>[3]</sup>. It is necessary to fabricate ferroelectric films directly on semiconductor substrate for MFS-FET. However, it is rather difficult to prepare a good ferroelectric film/Si interface because of the chemical reaction and the element interdiffusion<sup>[4]</sup>. In 1992,

Maffei and Krupanidhi<sup>[5]</sup> firstly proposed an insulating seeding layer inserted between the ferroelectric material and Si, resulting in a metal-ferroelectric-insulator-semiconductor (MFIS) structure.

The  $\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}$  (BNdT) films exhibit good ferroelectric properties compared with the conventional PZT films. BNdT films exhibit high remnant polarization ( $P_r$ ) of  $25 \mu\text{C}/\text{cm}^2$  and show a fatigue-free character<sup>[6,7]</sup>. The most important concern of ferroelectric materials in the nonvolatile memory is the built-in electric field in ferroelectrics-semiconductor interface due to the permanent polarization in ferroelectrics<sup>[8,9]</sup>.  $\text{Bi}_2\text{Ti}_2\text{O}_7$  (BTO) has a relatively high dielectric constant and low leakage current<sup>[10]</sup>. Thus, it can be used as a seeding layer between the ferroelectric films and semiconductor substrate to prevent the interface reactions<sup>[11,12]</sup>.

In this work,  $\text{Bi}_{3.54}\text{Nd}_{0.46}\text{Ti}_3\text{O}_{12}$  films and  $\text{Bi}_2\text{Ti}_2\text{O}_7$  seeding layer were fabricated by metalorganic solution decomposition, and the capacitance-voltage properties of the BNdT films without and with BTO seeding layer were investigated.

† Corresponding author. Prof., Ph.D.; Tel.: +86 451 86412133; Fax: +86 451 86413922; E-mail address: lzhen@hit.edu.cn (L. Zhen).

## 2. Experimental

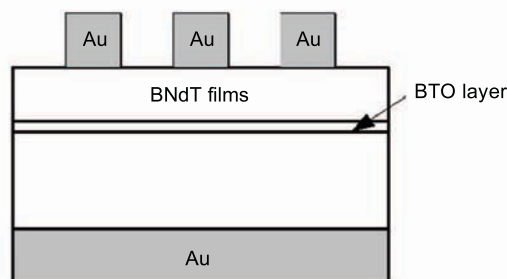
The BNdT films were prepared on n-Si(100) and BTO/n-Si(100) substrates using repeated coating/drying cycles. The precursor solutions of BNdT for the coating were synthesized from bismuth acetate, neodymium nitrate, and tetrabutyl titanate. Each solution contained 5% of excess bismuth nitrate due to the high volatile nature of bismuth. The BNdT films were spin coated onto the n-Si(100) and BTO/n-Si(100) substrates at 3000 r/min for 30 s to form a single layer. Each layer was then heated at 350°C in air for 10 min to remove residual organics. The deposition and heat-treatment procedures were repeated several times to obtain uniform layers with a thickness of 0.3  $\mu\text{m}$ . The final films were annealed at 680°C for 40 min in air. Similarly, the BTO layer was prepared from bismuth nitrate and tetrabutyl titanate<sup>[13]</sup> to form a  $\text{Bi}_2\text{Ti}_2\text{O}_7$  layer before coating the BNdT thin films.

The thicknesses of the BNdT and BTO films were 0.3  $\mu\text{m}$  and 30 nm, respectively. Au circular dots of cell area  $7.9 \times 10^{-3} \text{ cm}^2$  were deposited by DC magnetron sputtering through a shadow mask on the BNdT films as top electrodes, and Au film was sputtered on the back of the silicon substrate as bottom electrode to form an Au/BNdT/BTO/Si (MFIS) configuration (shown in Fig. 1) or Au/BNdT/Si (MFS) configuration. The crystallization of the BNdT films was examined by X-ray diffraction (XRD) using a Rigaku D/MAX- $\gamma$ A X-ray diffractometer (Japan). The surface morphology was analyzed by using a digital instrument multi-mode atomic force microscope (Nanoscope IIIa, USA). The capacitance-voltage ( $C$ - $V$ ) properties were measured using a LF impedance analyzer (HP4192A, Japan) at a frequency of 100 kHz.

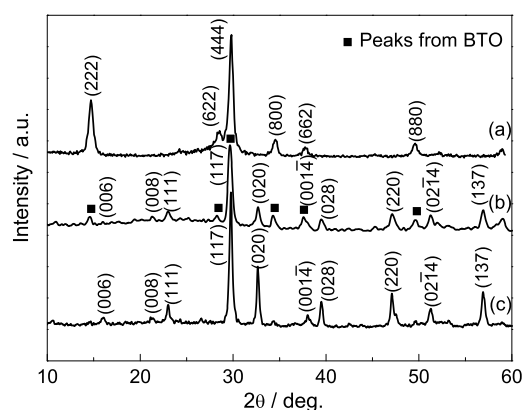
## 3. Results and Discussion

Figure 2 shows the XRD patterns of BTO, BNdT and BNdT/BTO films prepared on n-Si(100) substrates, respectively. The XRD pattern of the BTO films annealed at 500°C for 30 min (shown in Fig. 2(a)) has two stronger peaks of (444) and (222), which suggests that the films have a distinctly preferential (111) orientation<sup>[14]</sup>. Figure 2(b) and (c) are the XRD patterns of the BNdT/BTO and BNdT films annealed at 680°C for 40 min. The  $d$  values and intensities of the peaks of the BNdT films in the XRD pattern are essentially consistent with those given in JCPDS card #35-795 for  $\text{Bi}_4\text{Ti}_3\text{O}_{12}$ <sup>[15]</sup>.

The surface morphology of the BNdT and BNdT/BTO films was characterized with atomic force microscopy (AFM). Figure 3(a) and (b) show the two-dimensional and corresponding three-dimensional AFM images of BNdT and BNdT/BTO films, respectively. The AFM micrographs indicate that the films are all homogeneous with circular grains and



**Fig. 1** Schematic diagram of parallel-plate capacitor for measuring the electrical properties



**Fig. 2** XRD patterns of BTO (a), BNdT/BTO (b), and BNdT (c) films

no significant defects. The root-mean-square (RMS) value of the surface roughness of BNdT/BTO films (3.12 nm) is smaller than that of BNdT films (4.89 nm), and the average grain size of BNdT/BTO films (230 nm) is larger than that of BNdT films (170 nm).

The capacitances of BNdT films on Si substrate were measured to study the controllability of the Si surface potential. Figure 4 shows the typical capacitance-voltage ( $C$ - $V$ ) characteristic of BNdT films grown on Si substrate with a 0.1 V step at a frequency of 100 kHz under different bias voltages. The counterclockwise traces are clearly observed, as indicated by the arrows when the applied voltage increases from 1 to 2 V. But when the applied voltage further increases from 3 to 5 V, the  $C$ - $V$  curve shows a clockwise hysteresis loop, which is opposite to that from 1 to 2 V. No threshold hysteresis is apparent at 2.5 V.

Obviously, the  $C$ - $V$  curves in MFS structures all shift to the positive bias voltage compared to the reference metal-oxide-semiconductor (MOS) diode, which is due to the carrier traps and injection phenomena. We infer that a lot of crystalline defects which work as carrier traps exist near the interface between the BNdT films and Si substrate because of the lattice mismatch and the difference of thermal expansion between them. Some negative charges exist at the interface and they inject to BNdT films. Built-

Download English Version:

<https://daneshyari.com/en/article/1557009>

Download Persian Version:

<https://daneshyari.com/article/1557009>

[Daneshyari.com](https://daneshyari.com)