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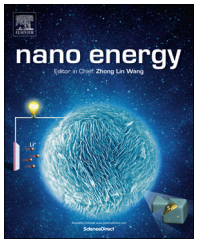

RAPID COMMUNICATION

Tuning thermal conductance across sintered silicon interface by local nanostructures

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Abstract
A large reduction of heat conduction through silicon-silicon sintered interface by local oxide nanostructures is quantitatively demonstrated by a newly developed method to directly measure thermal boundary conductance across bonded interfaces. Together with the theoretical analysis that relates the thermal boundary conductance to thermal conductivity of densely-packed bulk nanocrystalline silicon, we identify a route to significantly reduce the thermal conductivity from the state-of-art value, even to approach the amorphous silicon value. The finding is useful for designing nanostructured bulk silicon thermoelectrics.

Introduction

Thermoelectric materials, which can convert thermal energy directly to electricity, have attracted great interest as a mean for clean, silent, long-life, and ubiquitous waste-heat recovery. The performance of a thermoelectric material can be quantified by the dimensionless figure-of-merit $ZT=S^2\sigma T/(k_e+k_{ph})$, where S is Seebeck coefficient, σ is electrical conductivity, k_e and k_{ph} are thermal conductivity by electrons and phonons, and T is temperature. A successful strategy to enhance ZT has been to reduce lattice thermal conductivity without appreciably sacrificing the power factor $S^2\sigma$. For this, artificial nanostructuring has been particularly effective to inhibit heat conduction by scattering phonons at nanostructure-boundaries. Early studies on periodic nanostructures such as Bi_2Te_3/Sb_2Te_3 superlattice [1] and PbSeTe based quantum dot superlattice [2] marked high ZT, however, they have shortcoming in scalability and cost efficiency for practical applications. Recently, nanocrystalline materials (or nanostructured bulk composite), formed by compaction of nanopowder by sintering, have been demonstrated to be a promising mutual-adaptive solution for low thermal conductivity and high scalability [3-8].

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While thermal resistance at nanocrystalline grain boundaries plays a critical role for reducing thermal conductivity, little is known in experiment about to what extent the boundaries inhibit thermal transport, because thermal characterization of nanocrystalline thermoelectrics has been limited to measurements of effective thermal conductivity of the entire composite. Although there have been several numerical studies discussing causal relation between atomistic structure of a nanocrystalline grain boundary and its thermal boundary conductance (TBC) or resistance (TBR) [9,10], the modeling has been limited to ideal interfaces and is not sufficient to rigorously characterize complex boundary structures that arise in actual high-energy processes such as sintering. Therefore, an experiment to directly measure TBC of representative sintered interfaces is needed to understand the controllability of TBC by interface nanostructures. Such knowledge will open up the possibility to truly engineer phonon transport to further improve *ZT* of nanocrystalline thermoelectric materials.

Among various methods to measure thermal transport across solid interfaces, time-domain thermoreflectance method (TDTR) [11] utilizing transient reflectivity change has been widely used to measure TBCs in thin layered structures [12–14]. However, the method has not been applied to directly-bonded interfaces such as a sintered interface because the method is only applicable to highly planar and uniform interface located within thermal penetration depth from the heated surface (typically up to μm order). We have thus developed a process to fabricate a TDTR-measurable sample consisting of a silicon (Si) thin-film and Si substrate directly-bonded with highly planar and uniform interface. Here, we report TBC of sintered Si-Si interface, which serves as a model system for the interfaces in a sintered nanocrystalline silicon. The choice of material is encouraged by the recent progress in Si nanocrystalline thermoelectric [5,15], whose highest *ZT* is currently about 0.5 at 900 K. Further improvement of *ZT* would make Si-based thermoelectric a strong candidate for practical use with its high abundance, environmental friendliness, safety, and thermal stability.

By performing TDTR measurements of interfaces sintered at different temperatures, we identify the dependence of TBC on the interface structures. Here, we pay particular attention to the silicon oxide (SiO_x) nanostructures at the interface. SiO_x structures have been observed to precipitate at grain boundaries of sintered nanocrystalline silicon [15–17], and thus is a variable control parameter in the actual development of Si-based thermoelectrics. Furthermore, by combining the experimental results with a theoretical calculation that relates the value of TBC to the effective thermal conductivity of bulk nanocrystalline silicon, the current work reveals a great controllability of the effective thermal conductivity by interface structure from microscopic viewpoint.

Experimental method

A schematic diagram of the sample fabrication is shown in Figure 1. We have developed a process to fabricate a thin-Si/Si-substrate bonded structure that meets the above geometrical requisites by utilizing an SOI wafer and selective chemical etching. An SOI wafer consists of highly parallel and smooth three layers: thin-Si (SOI)/thin-SiO_2 (BOX)/handle. As in Figure 1, an SOI wafer and a Si wafer are cleaned with RCA and baked at 500 °C before bonding. After bonding, the handle Si and BOX were removed by etching with potassium hydrate (KOH) and hydrofluoric acid (HF), respectively, to obtain a thin-Si/Si-wafer structure.

For sintering, we used plasma activated sintering (PAS) (also known as spark plasma sintering) technique, which can effectively raise temperature and bond interfaces of materials by applying pulsed/direct current and mechanical pressure in vacuum [18]. As nano-powders are sintered inside a carbon (graphite) mold in a common fabrication process of nanocrystalline thermoelectrics, we placed 12×12 mm^2 SOI (Si 292 nm/SiO_2 400 nm/Si 675 μm) and Si chip face-to-face in the carbon mold. In the sintering process, we increased the temperature to the target value in 5 min and decreased it to ambient temperature in 7 min, applying constant pressure of 42 MPa and pulsed current for the initial 30 s followed by direct current. The interface structure was varied by changing the maximum sintering temperature (750–1100 °C) and the surface treatment of SOI and Si wafer before sintering. As for the surface treatment, we etched away the native oxide layers of SOI and Si wafer by HF for some samples to investigate the influence of the residual oxide layers. In addition, the matching of the crystal plane orientations was varied from SOI⟨1 0 0⟩/Si ⟨1 0 0⟩ to SOI⟨1 0 0⟩/Si⟨1 1 1⟩ to investigate the effect of lattice mismatch at the interface.

With the fabricated samples, TBC across the interface can be measured with TDTR. A Ti: Sapphire femtosecond pulsed laser (wave length: 800 nm, pulse width: ~100 fs and pulse rate: 80 MHz) is split into pump and probe. The pump beam, modulated at 11.05 MHz, is converted into blue beam (400 nm) with BIBO crystal, and heats the aluminum (Al) layer on the sample (Figure 1). The arrival timing of the probe beam is adjusted by a mechanical delay stage. The pump and probe $1/e^2$ radii at the sample surface are 30 μm and 5 μm, respectively. The aluminum acts as a heater, which absorbs pump

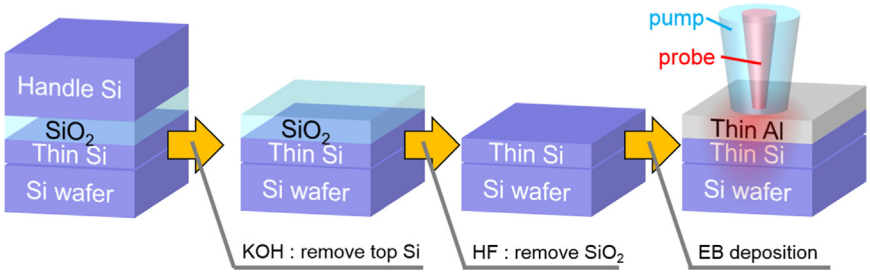

Figure 1 Schematic diagram of fabrication of thin-Si/Si-wafer bonded structure, and TDTR measurement.