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A model for statistical electromigration simulation with dependence on capping layer and Cu microstructure in two dimensions

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ABSTRACT

A model has been developed to simulate electromigration degradation in an interconnect segment in two dimensions using finite differences. The model was deployed on a parallel computer to statistically assess the lifetimes. The simulation takes into account the diffusion paths for electromigration mass transport along the grain boundaries and the capping layer. The microstructure is generated with a Monte Carlo algorithm, using a modified Potts model. Diffusivities along the grain boundaries and the capping layers were applied as multiples of a base diffusivity and were statistically scattered. The simulation results correlate well with electromigration tests.

1. Introduction

Although the end has been forecast for some time, Moore's Law [1] is still valid. The frontiers of what is technically, physically and economically possible have been successfully pushed forward. The current commercially available technology node is 14 nm and the trend towards smaller sizes will continue into the single digit nodes in the next 10 years. With every technology node, the major reliability challenges in the back-end-of-line (BEoL) stacks such as time dependent dielectric breakdown (TDDB), stress migration (SM) and electromigration (EM) are reiterated.

Studies in EM as the transport of conductor material under electric current stress have a history of about 50 years. They mainly started because of a shock to the semiconductor industry that this phenomenon has caused with accumulated unexpected chip failures in field operation. Through the transport of material in interconnects, mass depletion and accumulation occurs in critical places and the chip degrades [2,3]. In aluminum structures, owing to the stable oxide formation at the surface, EM was mostly a problem along grain boundaries of interconnects, which could be remedied by a bamboo microstructure with almost no grain boundaries aligned with the current flow direction. Prior to bamboo structures, diffusion along grain boundary paths was diminished with additives such as Cu [4]. The industry switched to copper interconnects in the late 1990s to reduce resistance and consequently the RC delay. With copper, dominant material transport takes place along the top capping layer interface [5]. Beginning with the 65 nm technology node, a bamboo microstructure cannot be maintained anymore [6]. Strengthening of the top interface with additional capping layers such as CoWP [7] resulted in the fact that EM along grain boundaries plays an increasing role. This work focuses on a model of EM incorporating the microstructure that enables statistical simulations to analyze interconnect segment failure times as a function of grain size in two spatial dimensions (2D).

The earliest work to model the development of mechanical stress due to EM goes back to Blech [8]. He determined a critical line length and electrical current density for EM to occur. Kirchheim et al. [9,10] derived equations of vacancy transport and stress development due to vacancy generation and annihilation. Shortly after, the popular work by Korhonen [11] appeared with his time dependent stress evolution equation which was later used in the EM simulation software MIT/Emsim [12], developed in the group of Thompson. Sarychev et al. [13] described a model that can determine all components of the stress tensor in three spatial dimen-

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sions (3D). EM in Al and Al–Cu interconnects was simulated by Park et al. [14]. A model similar to Korhonen's, but in terms of vacancy concentration was introduced by Clement and Thompson [15]. The physical model of Sukharev et al. [16–21] is used for simulating EM with the finite element method (FEM). The movement of a void in an interconnect was simulated by Bower and Shankar [22], also with FEM. Statistical simulations with FEM were done by Ceric and Selberherr [23], who ran many EM simulations to determine failure times of the modeled interconnects and its dependence on grain size. Other methods based on Monte Carlo simulations were proposed by Smy et al. [24] and Bruschi et al. [25].

The work in this paper is similar to Ceric's regarding statistical simulations of EM, but with a different approach. The mass balance equation with the EM vacancy flux was implemented in a 2D finite difference scheme. The microstructure of the interconnect segment is generated with a Monte Carlo method, namely a modified Potts model. Void nucleation and growth occurs in the simulation when a critical vacancy concentration is reached. The electrical resistance is monitored with a simple resistor model and fail times correspond to critical increases in resistance. Many simulations were run on a parallel computer to generate a suitable amount of statistics.

2. Simulation setup and procedure

2.1. Computational resource

The calculations were conducted on the Lonestar cluster at the Texas Advanced Computing Center of the University of Texas at Austin [26]. The Dell-Linux cluster consists of 1888 Dell PowerEdgeM610 nodes each containing two 3.3 GHz Xeon 5680 series hex-core processors making up a total number of 22656 cores. Despite the large resource, not more than 100 cores were used at any moment in time for the calculation described in this paper.

2.2. Computational domain

The simulation was carried out in 2D, and the computation domain is made up of a regular, equidistant grid with quadratic lattice cells. For the simulation, a grid size of 300 cells in the x-direction and 100 cells in the y-direction was used. By definition, the length of the cell edge was set to 1 nm. The computation domain represents a section of an on-chip interconnect segment parallel to the length-height plane, i.e. with the section normal parallel to the width dimension axis (z), which is outlined in Fig. 1.

2.3. Grain growth modeling

In order to obtain statistics for the EM simulation, a population of 100 interconnect segments was computed in parallel on the cluster. For the subsequent Monte Carlo simulation, a main random seed was specified before launching the 100 processes and each process set the individual seed to the sum of the main seed and the process identification number (process ID). The source of the random numbers was the pseudo random number generator from the GNU C library.

After launch of the 100 processes, the microstructure was generated firstly with an adaption of the Potts model [27,28]. The 300×100 grid cells were filled with random integers ranging from and including 1–30, representing pseudo-crystallographic orientations. As an estimation for a quasi-energy, each grid cell is assigned a number which is the sum of the unlike neighbors from the 8 Moore neighborhood cells. Schematics of Moore and von Neumann neighborhoods are pictured in Fig. 2. Moore neighbors outside the boundary were ignored. The intention of the Potts model is to minimize the total energy of the computation domain. In one Monte Carlo time step (MCS), in a permutated order each of the grid cells is given the chance to switch the pseudo-crystallographic orientation to a randomly chosen unlike Moore neighbor. If the energy decreases, the orientation is kept, otherwise the orientation is kept with the probability [29]

$$p = \exp(-2\Delta E), \tag{1}$$

where ΔE is the difference in energy before and after the orientation switch. The consequence of this procedure is the formation of domains with like orientations, mimicking grain growth in polycrystalline materials such as copper.

For a bamboo-like microstructure, i.e. grains spanning the full height (y-direction) of the interconnect segment model, the grain growth Monte Carlo simulation was run for typically 1000 MCS. For a more polycrystalline structure 300–500 MCS were used. Examples of grain structures for different MCS are shown in Fig. 3.

2.4. Diffusion modeling

After the microstructure generation, the grid cells belonging to diffusion paths were determined and indexed. By definition, the top line of grid cells was declared as a diffusion path, representing the top interface of the interconnect to the dielectric. The bottom interface, which serves as diffusion barrier, adhesion promoter and electric shunt layer, was not considered as a diffusion path in the simulation. Additionally, all cells with a Potts model energy other than zero, i.e. cells with unlike Moore neighbors regarding the pseudo-crystallographic orientation, were declared as diffusion active, representing the grain boundaries. By limitation of the equidistant quadratic grid with a cell edge length of 1 nm, the grain boundaries had generally a width of 2 cells for boundaries oriented parallel to the x- and y-direction and occasionally even 3 cells for diagonally oriented grain boundaries. Diffusion inside grains was neglected.

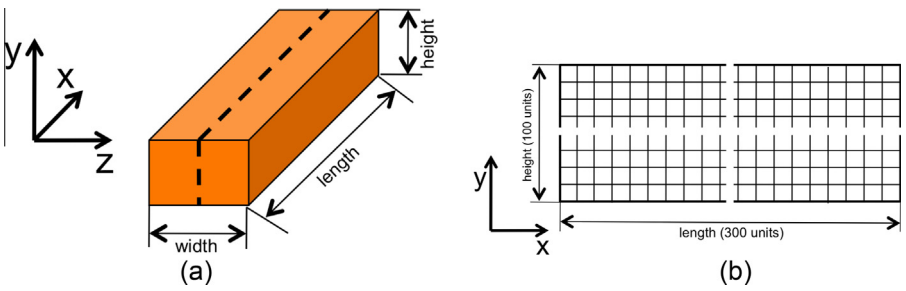

Fig. 1. (a) Illustrating the dimensions of the interconnect segment as used in the model. The dashed lines distinguish the section for the computation domain. (b) The computation domain dimensions. The length of one unit was by definition set to 1 nm.