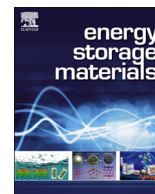




ELSEVIER

Contents lists available at ScienceDirect

Energy Storage Materials

journal homepage: www.elsevier.com/locate/ensm

Solid-state electric double layer capacitors for ac line-filtering

Han Gao^{a,1}, Jak Li^a, John R. Miller^{b,c}, Ronald A. Outlaw^d, Sue Butler^b, Keryn Lian^{a,*}^a University of Toronto, Toronto, Ontario, Canada^b JME Inc., Beachwood, OH, USA^c Case Western Reserve University, Cleveland, OH, USA^d College of William and Mary, Williamsburg, VA, USA

ARTICLE INFO

Article history:

Received 16 February 2016

Received in revised form

5 March 2016

Accepted 6 March 2016

Available online 31 March 2016

ABSTRACT

Ultra-fast solid electric double layer capacitors (EDLCs) have been developed in both sandwich and planar interdigitated configurations using vertically-oriented graphene nanosheet (VOGN) electrodes with a hydroxide ion-conducting tetraethylammonium hydroxide (TEAOH)–polyvinyl alcohol (PVA) polymer electrolyte. These solid-state EDLCs could be scanned at a rate of 1000 V s^{-1} in cyclic voltammetry and demonstrated response times of less than 1 ms. They retained high performance over 18 months of shelf storage and after 100,000 charge/discharge cycles with limited packaging, demonstrating the high stability of TEAOH–PVA electrolyte. The solid-state capacitors are capable of performing at elevated temperatures and have demonstrated a response time of 0.35 ms at 90°C . Given their ultra-fast rate capability, excellent shelf-life and cycle life, and excellent temperature stability, these solid-state EDLCs are promising smaller and lighter alternatives to the bulky electrolytic capacitors now used for ac line-filtering.

© 2016 Elsevier B.V. All rights reserved.

1. Introduction

In modern electronics, removing voltage fluctuations (rectification ripple) is necessary when converting alternating current (ac) to direct current (DC). Generally a capacitor is used for this purpose. The present solution for 120 Hz power filtering (double the value of the 60 Hz standard ac line frequency in the United States) is electrolytic capacitors. However, these devices are bulky and generally have low reliability.

Electric double layer capacitors (EDLCs), often referred to as supercapacitors or ultracapacitors, have much higher volumetric charge storage and high reliability compared with electrolytic capacitors and potentially allow for a size reduction. For an EDLC to be capable of efficient ac line-filtering, its impedance phase angle at 120 Hz must be near -90° . Typical EDLCs based on porous activated carbon electrodes perform poorly at this frequency and exhibit an impedance phase angle near 0° . This is primarily due to use of high-surface-area electrode material, which leads to distributed charge storage (porous electrode behavior) with a resulting response time of approximately 1 s.

* Corresponding author. Tel.: +1 416 978 8631.

E-mail address: keryn.lian@utoronto.ca (K. Lian).¹ Present address: Chemical Sciences and Engineering Division, Argonne National Laboratory, IL, USA.

Efficient ac line-filtering by an EDLC was first demonstrated in 2010 using vertically-oriented graphene electrodes [1]. Both series resistance and distributed charge storage were minimized to reach this level of performance. Since then, various materials, including carbon black, exfoliated graphene, reduced graphene oxide, activated reduced graphene oxide, graphene/carbon nanotube carpets, and others, have been used to achieve ac line-filtering performance [2–9]. Most of these studies used liquid electrolytes, which presents practical problems related to creating packaged, multi-cell EDLCs. Replacing liquid electrolytes with solid-state polymer electrolytes overcomes these practical problems needed to create next-generation EDLCs.

Earlier, we demonstrated a tetraethylammonium hydroxide (TEAOH)-based polymer electrolyte that outperformed widely-used KOH-based systems [10]. In this study, we leveraged this polymer electrolyte and vertically-oriented graphene nanosheet (VOGN) electrodes to demonstrate solid-state EDLC cells in both “sandwich” and planar interdigitated configurations. The TEAOH–polyvinyl alcohol (PVA) polymer electrolyte has relatively high ionic conductivity ($5\text{--}10 \text{ mS cm}^{-1}$), good film forming capability, and high environmental stability [10] while the VOGN electrodes exhibit minimum distributed charge storage behavior as well as low electronic resistance [1,11]. We combined the advantages of these two elements to achieve high-rate, solid-state EDLCs. The developed solid-state capacitors were

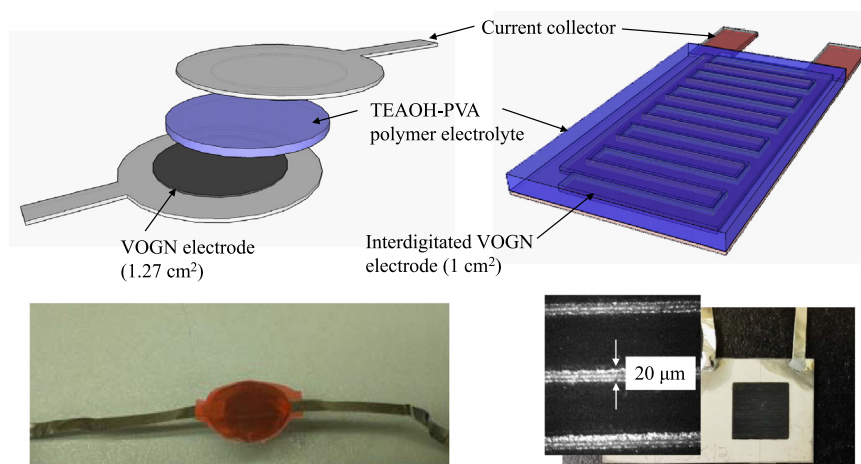


Fig. 1. Schematic diagrams of a solid-state sandwich design EDLC (left) and a solid planar interdigitated EDLC (right). Below the diagrams are pictures of the assembled devices.

tested at room temperature for shelf-life and cycle stability as well as high-temperature stability.

2. Material and methods

2.1. Preparation of TEAOH–PVA polymer electrolyte

A polymer electrolyte precursor solution was prepared by mixing 5% PVA (MW=145,000) aqueous solution and a TEAOH solution at room temperature. Based on our previous study, an optimized TEAOH–PVA electrolyte composition of ca. 81 wt% TEAOH and ca. 19 wt% PVA was used [10].

2.2. Preparation of VOGN electrodes and construction of solid cells

The electrodes were VOGN grown on Ni by microwave plasma enhanced chemical vapor deposition on either round disks or rectangular plates [11–13]. Both solid-state sandwich and solid-state planar interdigitated EDLCs were fabricated as shown in Fig. 1. In the latter case, laser ablation was used to cut a 20- μm -wide gap through the VOGN and the 1- μm thick nickel current collector below it. The planar cell capacitance at 120 Hz was 30–35 $\mu\text{F cm}^{-2}$ for an electrolyte of 1 M tetraethylammonium tetrafluoroborate salt in acetonitrile or propylene carbonate solvent [13].

The solid-state sandwich cell was constructed using the following steps: (i) The electrolyte precursor solution was coated onto the VOGN round disks electrodes via solution casting. (ii) Two electrolyte-coated electrodes were fused together for 20 min at ambient temperature under 20–30 kPa pressure. (iii) An insulating tape was applied to cover the cell for protection. Typical VOGN spacing is ca. 200 nm and the height ca. 1 μm . The geometric area of the electrodes is 1.27 cm^2 .

The solid-state 1 cm^2 planar interdigitated EDLC was constructed by drop casting a measured volume of polymer electrolyte precursor solution onto the electrode surface. The water from the precursor solution was allowed to evaporate at room temperature, forming a polymer electrolyte layer covering the interdigitated pattern (Fig. 1).

2.3. Electrochemical characterizations

All cells were characterized using cyclic voltammetry (CV), galvanostatic charge/discharge (GCD), and electrochemical impedance spectroscopy (EIS). CV and GCD was performed either using

a CHI 760D bipotentiostat or an EG&G PAR 263A potentiostat/galvanostat. EIS was performed using a Solartron 1255 frequency response analyzer interfaced with the EG&G 263A. The EIS spectra were recorded from 100 kHz to 1 Hz with 5 mV amplitude under zero-volt bias. Unless otherwise specified, electrochemical experiments were carried out at room temperature.

For the shelf-life study, the solid-state cells were stored in a controlled condition of 25 $^{\circ}\text{C}$ and 45% ($\pm 3\%$) relative humidity. A temperature/humidity chamber (Espec SH-241) was used to conduct thermal stability tests from 25 to 100 $^{\circ}\text{C}$ (10 $^{\circ}\text{C}$ interval, 50% relative humidity) with a 30 min equilibrium time at each temperature.

3. Results and discussion

Detailed structure and morphologies of the VOGN were reported previously [1,11–13]. Characterizations of the solid-state sandwich EDLC focused on its rate capability, cycle life, and shelf life. Studies on a solid-state planar EDLC focused on performance at higher temperatures.

3.1. Solid-state sandwich EDLC

The CVs (normalized by capacitance) of the solid-state sandwich EDLC at different scan rates are depicted in Fig. 2a. All CVs showed a near rectangular profile. The device was able to charge and discharge at an ultra-high rate of 1000 V s^{-1} . At this rate, the EDLC exhibited a capacitance of ca. 80 $\mu\text{F cm}^{-2}$, 65% of the capacitance at 1 V s^{-1} . Although the profiles of the solid-state device appeared slightly tilted with increasing scan rate, the combination of easily accessible VOGN electrodes (especially on the edge plane of the graphene sheets) and the highly conductive TEAOH–PVA polymer electrolyte enabled extremely fast ion transport.

Charge/discharge curves of the solid-state sandwich EDLC under different current densities are shown in Fig. 2b. The linearity and symmetry of the curves confirmed the capacitive nature of the device, in good agreement with the CV results (Fig. 2a). Also shown in Fig. 2b is the discharge capacitance calculated from the slope of the discharge curves. For example, the capacitance was 119 $\mu\text{F cm}^{-2}$ under a current density of 0.39 mA cm^{-2} . A ten-fold increase in current density led to only a 10% reduction in capacitance. More importantly, the extremely small charge/discharge times in the range of milliseconds demonstrated the rapid charge/discharge characteristics of this solid-state EDLC.

The cycling stability of the solid-state EDLC was investigated using GCD and EIS. Nyquist plots of the capacitor before and after

Download English Version:

<https://daneshyari.com/en/article/1564595>

Download Persian Version:

<https://daneshyari.com/article/1564595>

[Daneshyari.com](https://daneshyari.com)