

Effects of Ag content on fracture resistance of Sn–Ag–Cu lead-free solders under high-strain rate conditions

Daewoong Suh^{a,*}, Dong W. Kim^b, Pilin Liu^a, Hyunchul Kim^a, Jessica A. Weninger^a, Chetan M. Kumar^a, Aparna Prasad^a, Brian W. Grimsley^c, Hazel B. Tejada^a

^a Technology and Manufacturing Group, Intel Corporation, Chandler, AZ 85226, United States

^b Flash Memory Group, Intel Corporation, Folsom, CA 95630, United States

^c Flash Memory Group, Intel Corporation, Chandler, AZ 85226, United States

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Abstract

Effects of Ag content on fracture resistance of Sn–Ag–Cu solders under high-strain rate conditions are examined in an attempt to optimize bulk properties of solders for enhanced drop performance. The concept of extrinsic toughening is invoked for alloy design. High bulk compliance and plastic energy dissipation are identified as key factors to enhance fracture resistance under high-strain rate conditions. Systematic changes of Ag content in Sn–Ag–Cu solders are made to modulate bulk compliance and plastic energy dissipation ability of Sn–Ag–Cu solders. Low-Ag alloys are found to have both high bulk compliance and high plastic energy dissipation ability. As a result, low-Ag alloys are found to exhibit significantly higher fracture resistance under high-strain rate conditions on electrolytic NiAu surface finish. No significant difference in interfaces between high-Ag and low-Ag alloys is found in terms of thickness, chemistry, and grain size of $(\text{CuNi})_6\text{Sn}_5$ and $(\text{NiCu})_3\text{Sn}_4$ intermetallic compound layers. The observed enhancement of drop performance of low-Ag alloys is therefore attributed to increased bulk compliance and plastic energy dissipation ability through increased primary Sn phase.

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1. Introduction

Near-eutectic Sn–Ag–Cu (SAC) alloys are widely used as lead-free solutions for the ball-grid-array (BGA) interconnect (i.e., package-to-board interconnect) in the microelectronic packaging industry. The industry standard Sn–Ag–Cu alloys such as Sn–14 wt.%Ag–0.5 wt.%Cu (SAC405) or Sn–3 wt.%Ag–0.5 wt.%Cu (SAC305) alloys; however, exhibit significantly poorer performance than eutectic SnPb under high-strain rate conditions such as drop testing [1]. (In this article, drop testing refers to a high-gravity shock testing typically conducted for cellular or handheld devices. The most common testing setup involves the g-force of 1500 G and duration of 0.5 ms [2].) With fine BGA interconnect geometries such as pitches of 0.5 mm or less, SAC405 or 305 alloys frequently show orders-of-magnitude poorer performance than eutectic SnPb in

the drop testing. With the industry-wide trend towards “mobility” or “ultra-small form factor”, this low drop performance of SAC405 or 305 alloys is and will continue to be a major issue in drop-critical areas such as cellular and handheld applications [3,4]. In order to address this challenge, drop-resistant SAC alloy development efforts have been launched by the current authors and, over the past years, considerable progress has been made in this area. In this article, effects of bulk properties on high-strain rate fracture resistance of SAC alloys are presented. Specifically, Ag content is controlled to modulate bulk properties of SAC alloys. It is found that bulk properties of SAC alloys have profound effects on high-strain rate fracture resistance and lowering Ag content is found to be highly effective in increasing bulk compliance and plastic energy dissipation ability, resulting in significant performance enhancement in drop testing.

2. Experimental procedure

Scheil solidification simulation was conducted in Thermocalc (Thermocalc software AB) with NSLD2 Solder database

* Corresponding author at: 5000 West Chandler Boulevard, CH5-159, Chandler, AZ 85226, United States. Tel.: +1 480 552 4108; fax: +1 480 554 1521.

E-mail address: daewoong.suh@intel.com (D. Suh).

(developed by National Physical Laboratory, Teddington, UK). Dog-bone shaped tensile specimens with nominal gauge length of 50 mm and thickness of 3.2 mm were water-jet machined from the commercial-grade solder plate. Uniaxial tensile testing was conducted at the constant strain rate of $5 \times 10^{-4} \text{ s}^{-1}$ in order to obtain strength and elongation values. Elastic modulus (Young's modulus) was measured by ultrasonic stress wave propagation method where the velocity of a longitudinal stress wave through rectangular specimens (approximately 15 mm in thickness) was measured. Commercially available solder spheres with diameter of 0.3 mm were placed on commercially available electrolytic NiAu surface finish after water-soluble flux application and reflowed with a nominal peak temperature of 245 °C. The interface between solder spheres and surface finish was examined with SEM and EDX. Solder bulk was removed through chemical etching in nitric acid to expose the top layer of intermetallic compound (IMC) for grain size and morphology examination. TEM samples were prepared by lift-out method under FEI Dual-Beam DB-235 focused ion beam (FIB). The solder/surface finish interface was then examined in a JEOL 2010 F transmission electron microscope operated at 200 kV. The test vehicle used for drop testing was 14 mm × 14 mm × 1 mm in size with 456 solder spheres (0.3 mm in diameter) reflowed on electrolytic NiAu surface finish at a 0.5 mm pitch. The printed wiring board used in this study was 132 mm × 77 mm × 1 mm in size with 15 total units surface-mounted on OSP (organic solderability protection) surface finish (Fig. 1). After assembly, the assembled test vehicle and board was tested according to the JEDEC standard drop testing specification for handheld application [2]. The JEDEC standard drop test is a free-fall shock test requiring an acceleration profile of 1500 G peak acceleration, 0.5 ms duration in a half sine profile (Fig. 2). During the test, electrical data was collected for all 15 units on the board using an in-situ event detector data acquisition system capable of sampling at a minimum of 50 kHz to capture any failures during drop testing. This drop test controls the input acceleration to the test board, and the output board deflection/displacement (and related strain rate on the package test vehicle) was captured as an electrical response using the event detector specified above. After testing was completed the electrical data was confirmed through post-testing failure analysis.

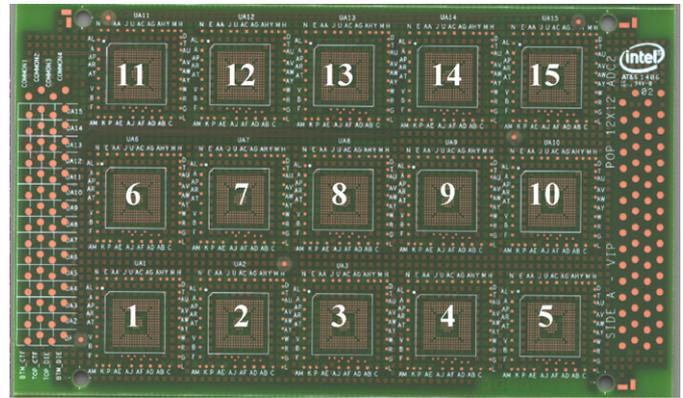


Fig. 1. Schematic diagram of JEDEC standard test board as specified in JESD22-B111.

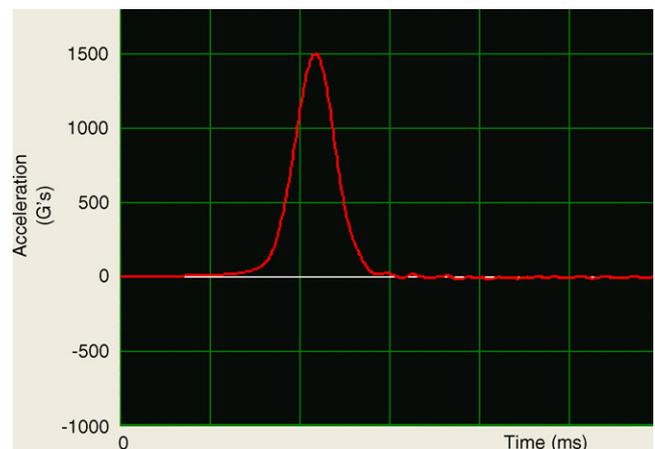


Fig. 2. Representative half sinusoidal profile of 1500 g with 0.5 ms.

3. Results and discussion

3.1. Underlying concept for alloy design

The main failure mode as a result of drop testing is found to be crack propagation along the interfaces (solder/IMC, IMC/IMC, IMC/base metal, etc.) formed at the solder joint (Figs. 3 and 12). The outstanding question is whether “bulk” properties of solder can be optimized to suppress or delay this essentially “interfa-

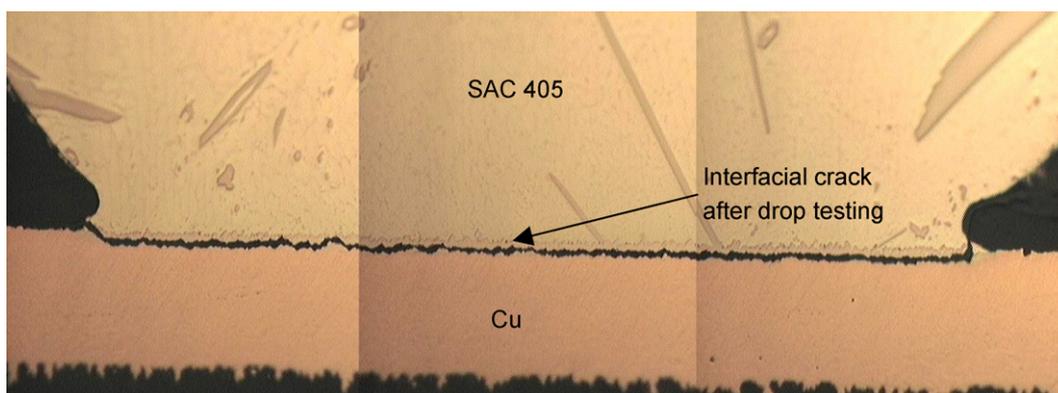


Fig. 3. Representative failure mode in SAC alloys during drop testing.

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