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Implementation of carbon nanotube bundles in sub-5 micron diameter through-silicon-via structures for three-dimensionally stacked integrated circuits

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ABSTRACT

Carbon nanotubes (CNT) are being intensely investigated and explored as an alternative to the use of traditional metals in the interconnects for 3D chip-stacking, because of its numerous advantageous properties, in particular high thermal and electrical conductivity that are several times higher than of any comparable metal. In this work, we have successfully implemented growth and realized functional integration of multiwalled-CNT bundles in sub-5 μm diameter, high-aspect ratio 'Through-Silicon-Vias' (TSV). Large-area growth of CNT bundles was realized in TSVs on top of metal-lines in a bottom-up approach, at complimentary-metal-oxide-semiconductor processing-compatible temperatures. An innovative approach for minimization of the interfacial-barrier contact resistance between CNT and metal-lines was adopted, by introducing an alloy of Al-rich Al_2O_3 as catalyst-holding layer, instead of conventional 10 nm. Good electrical-contact between metal-lines to CNTs is observed. A repeatable, non-destructive approach was used for electrical characterization studies of CNT-TSVs. The combined electrical resistance of an individual CNT-filled TSV was found to be ~1.2 kΩ. Issues related to selective deposition of Fe-catalyst thin-film at the TSV-bottom, and growth of the CNTs from TSV sidewalls were solved by novel approach of wafer-to-wafer bonding. Structural investigations proved that as-grown CNT bundles are anchored robustly in the metal-layers.

1. Introduction

As the complexity and functionality of very large scale integration (VLSI) architectures continues to increase significantly, there is an imminent need for convergence of on-chip interconnects and packaging for optimization of circuit performance in terms of signal transmission, power consumption and form-factors [1]. Three-dimensional (3D) chip integration allows access to novel architectural pathways to miniaturization, higher bandwidth, low-power, high performance and system-level scaling. Integration options include vertically-stacked die and/or silicon interposer, depending on the specific application needs. Currently, 'Through Silicon Via' (TSV) technology is rapidly evolving as a key-enabling solution to challenges of 3D integration. 3D TSV interconnects approach is an attractive way for empowering "More than Moore" novel applications because they provide technical solutions which allow heterogeneous assembly of multiple, disparate dies to form a stacked-die micro-system. With the International Technology Roadmap for Semiconductors (ITRS) 2012 guidelines [2] in mind, the ultimate goal is to integrate heterogeneous technologies such as digital, analog, RF, and micro-electromechanical systems (MEMS) onto one single platform; inevitably, TSV interconnects are bound to play a major role in making this goal feasible. 3D TSV based interconnects not only provide for reduction of physical size for VLSI structures thus saving valuable real-estate, but they also allow for faster operating speeds and low power operation of integrated circuits (IC). The short interconnect lengths improves clock-rates, lowers power consumption, minimizes local and global delays, and reduces the need for large input/output drivers [3,4]. In future, speed of signal transmission and degree of signal integrity through the interconnects based on TSV technology in VLSI architectures, are going to be the most important deciding factors for 3D-ICs commercial success.

The 2012 market research report [5] by "Yole Developpement" firm reveals that 3D-TSV chips will occupy 9% of the semiconductor

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market in 2017. 3D-IC which typically uses TSV "via middle" process for memory and logic IC stacking is expected to grow the fastest in wafer production as well as in the overall value. As per their analysis, 2015 would mark a key turning-point for the first, wide-scale implementation of 3D-IC technology in significant volume, for instance, driven by the commercialization of the hybrid memory cubes of Micron, Samsung, SK-Hynix and IBM in server and high-performance computing (HPC) markets. The outlook is quite bright for the future 'virtual integrated device' manufacturers (IDM) model, that is poised to expand the 3D-IC chip business by great margin. The market-value of the total manufacturing output estimated in the report for the global 3D TSV semiconductor packaging business, and assembly and test markets is bound to reach $8 Billion in capital value by 2017, out of which around $3.8 Billion will be related to the middle-end wafer processing activity such as TSV etching, filling, wiring, bumping, wafer testing and wafer-level assembly. The widespread applications of the 3D-IC technology makes it highly attractive for applications in more than 80 types of electronic ICs (from GPUs, FPGAs, sensors, RF chips, power devices, etc.), and could be implemented in more than 90 different end-products such as smart-phones, smart TV, game stations, servers, pace-makers, data-centers, electronics for electric-vehicles, etc.

For the semiconductor and electronics industry to continue with its drive for downscaling, industry would have to look for novel ways, new designs, and charter new technological pathways in the realm of process engineering. In this perspective, downscaling of the TSV dimensions is one of the most important goals. Interconnect scaling would allow facile connectivity between different blocks of lower-level of BEOL metal-lines in vertical stacked dies, and thus enhance the packaging density. It is understandable that due to scaling of TSV interconnects, resistivity of the metals such as copper, used for via-filling, increases rapidly. In this aspect the proper choice of via-filling materials is highly important. Upto now, conventional filler materials, such as copper (Cu), tungsten (W), doped poly-silicon, gold (Au), and conductive polymer pastes, have been utilized widely for few years. However, each of these have their own technical, performance, and other limitations that present significant challenges to fabrication, packaging, and testing engineers, and overall manufacturing in broader perspective.

The desirable properties of more suitable via-filling materials are high current carrying capability, lower thermo-mechanical or thermo-electric stress effects during operation, void-free filling, and good thermal cycling performance. High electrical conductivity, a well-established electrochemical deposition (ECD) process, and good thermal characteristics make Cu an obvious choice as a filler material for TSV. Despite these features, (a) limitation of non-conformal seed-layer deposition, required for further ECD process, (b) catastrophic defects caused by electro-migration at high current-densities, (c) increasing grain-boundary resistivity caused by the combination of increased scattering, (d) presence of highly diffusive barrier-layer, (e) and creation of voids under physical-scaling, all together reveal that choice of Cu as a filler-material in high aspect-ratio (AR) TSV vias is a compromised one [2]. Similarly, W is best suited to fill only small-length, small diameter vias, and has much lower conductivity than Cu. Likewise, poly-silicon, Au, and other materials have similar, and other/additional issues that make them unsuitable as interconnect filler-materials.

Thus, inevitably, active research and development work are being pursued in academia and industry for identifying and developing appropriate filler materials for application in low-dimension and high-AR TSVs based inter-chip interconnects, that offers desirable physical, chemical, mechanical, thermal and electrical properties. On this front, carbon nanotubes (CNTs) bundles are highly attractive candidate as potential filler-material, which hold the technical-promise to overcome the traditional bottlenecks associated with TSV interconnects. The most promising advantages of CNTs arise due to (i) their capacity for sustaining high current-densities $\sim 10^9$ A/cm^{2}in single CNT, (ii) low grain-boundaries, i.e., low internal-scattering resistance, (iii) high thermal-conductivity (1750–5800W·mK^{-1}), which exceeds that of copper (400W·mK^{-1}) by as much as 15 times, and is therefore ideal for dissipating heat from active hotspots to heat-sinks, and (iv) low-coefficient of thermal expansion (CTE), $\pm 0.4\times 10^{-6}$/K, as compared to the Cu (17.5×10^{-6}/°C), or Si (2.5×10^{-6}/°C). The low-CTE values of CNTs lend them huge advantage in terms of generation of lowest-possible thermo-mechanical stress effects in the vicinity of TSV structures [6,7]. Since the past few years, there has been a strong motivation for the researchers to implement CNT technology simultaneously, into both on-chip interconnects (BEOL) and inter-chip interconnects (TSV). Kawarada et al. [8,9] have shown that the CNT bundles can be successfully grown on top of metal-lines inside of SiO_2 vias (BEOL) of diameter as low as $\sim$2 μm, with CNT growth density of 1.6×10^{11} cm^{-2} at 390 °C. They demonstrated that after chemical mechanical polishing (CMP) the resistance of CNT bundle falls from 32 Ω to 0.9 Ω, which is possibly due to contributions by all of the interior walls of MWCNT to the overall bundle-conductivity. Furthermore, a many-fold enhancement of the as-grown CNT bundle density, to an order of magnitude higher value (2.5×10^{12} cm^{-2}), has also been demonstrated [10] via wet-chemical densification process. The reported process of densification led to characteristic advantages, such as reduction of the via resistance down to 22 Ω for about 1000 CNTs embedded in vertical interconnects of AR $\sim$4, and with 250 nm diameter.

However, in general, the determination of the total bundle resistance in a TSV via, is made by estimating the number of CNTs in a given area by visual inspection under SEM, which is not an accurate approach. Alternatively, a relatively more accurate determination of the total number-density of the CNTs, in any given TSV via, can be made by making electro-chemical contacts [11]. Here, CNT bundles are grown atop metal-lines followed by CMP, and metal-electroplating accomplished by metal-ion-reduction at highly-reactive, dangling CNT tips. In this way, electro-pads are formed only on those CNTs that are in electrical contact with the bottom metal-lines. Compared to the previous approach, this is a relatively more accurate method to determine the density of truly conductive CNT inside any particular via. Even further, another way to extract precise value of CNT-bundle resistivity [12] is to deposit an oxide-layer embedding the protruding CNT-bundle, followed by CMP and pad formation. The via-resistivity was measured to be 2.7×10^{-3} Ω·cm for SiO_2 via of 300 nm diameter and 530 nm depth. Subsequently, they transferred and replicated the same technology to 150 nm diameter interconnects [13], which is advantageous and compatible with the single Cu damascene module at 130 nm technology node.

On the other hand, for inter-chip interconnects technology through the implementation of TSVs, the preferred diameters, and the length comes in the range of 30–50 μm and 85–200 μm, respectively [14,15]. The resistance of the CNT-bundle in the TSV vias depends directly on the CNTs length; for instance, as the length increases from 86 μm to 139 μm, the resistance increases from 0.21 kΩ to 0.34 kΩ, respectively. The CNT growth and via-filling in TSV technology can be accomplished by two distinct process-flows, viz., (i) growth of CNT bundles directly in TSV-via in a bottom-up approach, or (ii) post-growth transfer of CNT bundles to the TSV vias [16–19]. It has been observed that bottom-up approach of CNT growth requires high growth temperatures, approximately 700 °C for longer TSV channels [14]. At the same time, the post-growth transfer process is limited to large-diameter TSVs ($\phi > 30$ μm) only due to problems with the alignment accuracy [16]. Currently, it is quite an intricate technical challenge to transfer the CNT bundles efficiently into TSVs with $\phi < 5$ μm, due to unavoidable misalignment error of $\sim$2 μm. Thus for small-diameter and high aspect-ratio