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Carrier density distribution in silicon nanowires investigated by scanning thermal microscopy and Kelvin probe force microscopy

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ABSTRACT

The use of scanning thermal microscopy (SThM) and Kelvin probe force microscopy (KPFM) to investigate silicon nanowires (SiNWs) is presented. SThM allows imaging of temperature distribution at the nanoscale, while KPFM images the potential distribution with AFM-related ultra-high spatial resolution. Both techniques are therefore suitable for imaging the resistance distribution. We show results of experimental examination of dual channel *n*-type SiNWs with channel width of 100 nm, while the channel was open and current was flowing through the SiNW. To investigate the carrier distribution in the SiNWs we performed SThM and KPFM scans. The SThM results showed non-symmetrical temperature distribution along the SiNWs with temperature maximum shifted towards the contact of higher potential. These results corresponded to those expressed by the distribution of potential gradient along the SiNWs, obtained using the KPFM method. Consequently, non-uniform distribution of resistance was shown, being a result of non-uniform carrier density distribution in the structure and showing the pinch-off effect. Last but not least, the results were also compared with results of finite-element method modeling.

1. Introduction

Along with the expansion of semiconductor industry and the development of manufacturing technology of integrated circuits new diagnostic methods have been continuously emerging. However, as a result of miniaturization the final devices have become extremely complex, so that the *in situ* investigation of many of them has turned out to be impossible. Therefore, finite-element method (FEM) modeling techniques replaced standard experimental methods at the nanoscale *e.g.*, in evaluating the carrier density distribution or heat flow in working semiconductor devices. Nevertheless, experimental confirmation of modeled phenomena is always desirable and should strengthen the FEM usability. Moreover, linking empirical results to modeled ones should enable establishment of new diagnostic methods, which can be later used in evaluation of newly constructed nanodevices.

Predictions of the behavior of metal-oxide-semicondutor field-effect transistors (MOSFETs), compared with results of standard electrical investigations, have been published since 1960s (Sah, 1964), accompanied with the analyses of the pinch-off effect present in the channel of such transistors (Booth and White, 1984; Reddi and Sah, 1965). However, for a long time any direct investigation of these devices and effects was not possible due to closed construction and lack of high-resolution experimental methods. Attempts were made in early 1990s with use of micro-Raman spectroscopy (Ostermeir et al., 1992), spatial resolution of which was still not sufficient. Introduction and development of scanning probe microscopy methods provided means to *e.g.*, map the temperature distribution in a MOSFET, which could be connected to its electrical properties (Aubry et al., 2007; Hendarto et al., 2005; Lai and Majumdar, 1996); however, these maps and profiles could be still affected by the standard construction of the transistor, having the channel covered by the gate electrode. Moreover, the results of nMOSFET investigations by SThM, shown by Hendarto et al. (2005) are described by those authors as only possibly being explained by the pinch-off effect, as no comparisons enabling further conclusions were presented. In addition to transistors, in past 10 years vari-

Abbreviations: SThM, scanning thermal microscopy; P-SThM, passive-mode scanning thermal microscopy; KPFM, kelvin probe force microscopy; AFM, atomic force microscopy; SiNW, silicon nanowire; FEM, finite-element method; (MOS)FET, (metal-oxide-semiconductor) field-effect transistor.

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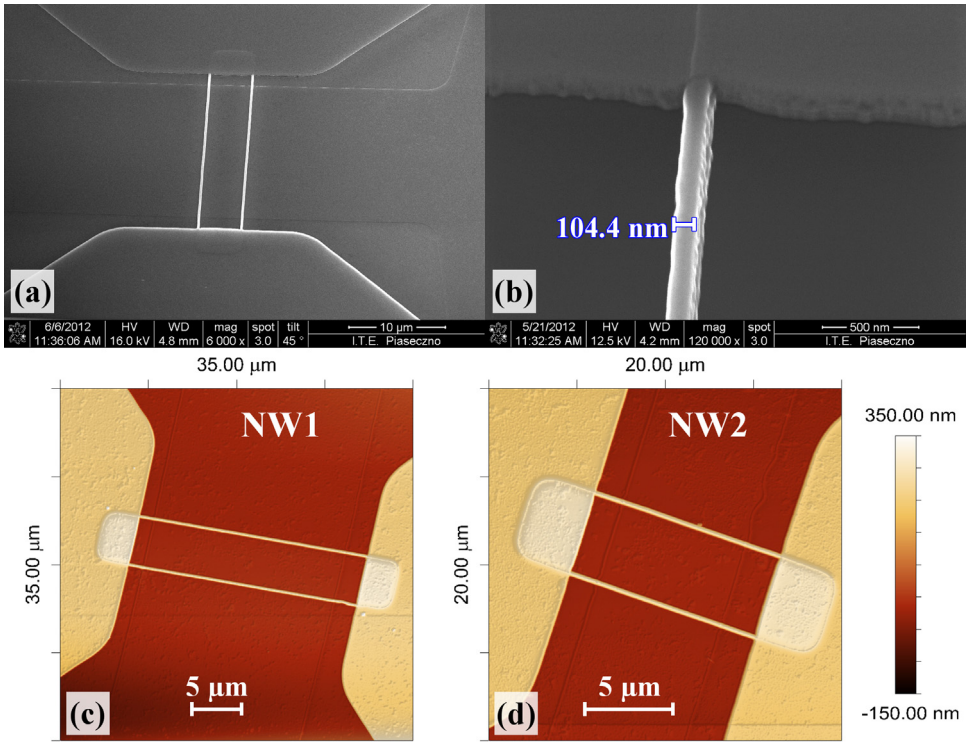

Fig. 1. (a) SEM image of a NW2-type nanowire, (b) bare SiNW before the deposition of silicon nitride layer, (c and d) tapping-mode AFM images of the investigated nanowire structures.

ous types of semiconductor nanowires have been investigated with regard to their electrical (Fan and Lu, 2005; Lee et al., 2012; Mody et al., 2008; Tsai et al., 2011) and, separately, self-heating properties (Karg et al., 2013; Menges et al., 2012; Puyoo et al., 2011; Soudi et al., 2011). Moreover, the development of new types of transistors and the basic physical investigation require advanced modeling of the semiconductor structures (Cahill et al., 2014; Kolluri et al., 2007; Pop et al., 2006, 2005).

In the paper, we present results of investigations of silicon nanowires, carried out using scanning thermal microscopy (SThM) and, as a supporting method, by Kelvin probe force microscopy (KPFM). These two methods are based on atomic force microscopy (AFM) and enable simultaneous imaging of surface topography and, respectively, surface temperature map and surface potential distribution. The main advantage of both methods is that they provide sub-micrometer resolution, basically in the range of tenths of nanometers (Shi et al., 2001; Zerweck et al., 2005). Hence, detailed imaging along a nanowire is possible. Both temperature and potential gradient are linked to the local resistance of a working nanowire (*i.e.*, with current flowing through it). Therefore, based on the temperature and potential maps, the carrier density distribution along the nanowires can be shown qualitatively. In the paper we present results revealing the pinch-off effect, which is confirmed by results of FEM modeling of the investigated structures.

2. Fabrication of silicon nanowires

The silicon nanowires were manufactured using CMOS-compatible pattern definition by edge oxidation (PaDEOx) process, developed in ITE Warsaw (Zaborowski et al., 2009). In this process the SiNWs were first etched in SOI *p*-type wafers using plasma Bosch etching process and a SiO_2 hard mask. Secondly, the *p*-type 100 nm wide nanowire structures were overcompensated to *n*-type by doping with phosphorus ions. Afterwards, 14-nm thermal oxide layer was grown and a 14-nm thin layer of silicon nitride

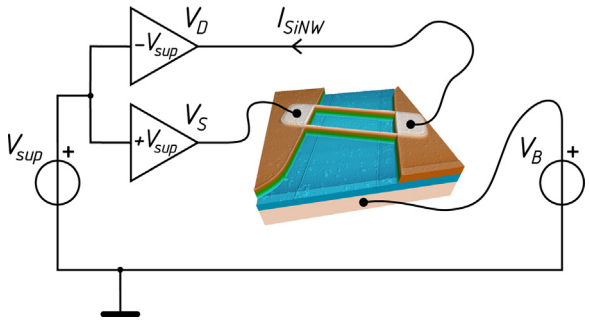

Fig. 2. Electrical connections to the SiNW; please note bulk acting as a gate.

was deposited in LP-CVD process. The fabrication process of the SiNWs was thoroughly described elsewhere (Zaborowski et al., 2012). Eventually, the electronic structure of the SiNWs could be described as $n^+ - n - n^+$ junction-less FET with the Si handle wafer acting as a back gate electrode. In Fig. 1a and b, the SEM images of the SiNWs are presented, showing the general view of the structure and a close-up of a SiNW.

In the presented experiments, two types of nanowires have been investigated. Let NW1 indicate nanowires that were 23 µm long and had 100 nm in width, while NW2–nanowires with length of 11 µm and width of 100 nm as well. The thickness of both NW1 and NW2 was 160 nm. For reference, tapping-mode AFM images of the investigated structures are shown in Fig. 1c and d.

3. Experimental set-up

3.1. AFM-based experiments

The experiments involving use of scanning thermal microscopy and Kelvin probe force microscopy were carried out using a Veeco Nanoman VS atomic force microscope with a Nanoscope V con-