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Low programming voltage resistive switching in reactive metal/polycrystalline $Pr_{0.7}Ca_{0.3}MnO_3$ devices

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ABSTRACT

The resistive switching (RS) characteristics of Pt/$Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO)/W devices with a submicron via-hole structure are investigated. Reproducible and stable switching behavior was achieved in voltage sweeping cycles, while the resistance change was more than two orders of magnitude. No forming process was required to induce the RS. Detailed current density–voltage analysis suggest that the oxidation and reduction reaction of an interfacial WO_x layer by electrochemical migration of oxygen between the W bottom electrode and the PCMO layer plays a crucial role in the RS of the Pt/PCMO/W structures Furthermore, the relatively low programming voltage (±1.5 V), which is significantly less than the values previously reported in chemically reactive metal/PCMO devices, might be ascribed to the thermal-assisted RS and the unique properties of W metal and its oxides in nano-scale devices.

1. Introduction

Resistive random access memory (RRAM) holds great promise as a next-generation non-volatile memory device on account of its excellent scalability, low power consumption, and nondestructive readout [1–3]. As a consequence, the resistive switching (RS) of thin films of the manganite perovskite, $R_{0.7}Ca_{0.3}MnO_3$ (R = Pr, La), sandwiched between the top electrode (TE) and the bottom electrode (BE) has been the focus of extensive research [3–17]. Although many models have been proposed to elucidate the RS mechanism, such as the space charge limited current (SCLC) [5], oxygen migration [6], and the Schottky barrier [3,7,8], none of them can provide a fully self-consistent explanation of all the observed physical phenomena. Recent studies have shown that metallic electrodes play a crucial role in determining the characteristics of the RS behavior, such as the switching polarity and speed [11]. On the other hand, the redox reaction taking place between a chemically reactive metal (M = Al, Ti, Ta, or Sm) and manganites is considered as an essential condition for RS [9–17]. By utilizing the nano-scale interface switching of manganites, the performance of Al/PCMO memory devices has been significantly improved; this improvement has taken place not only in their switching speed and uniformity but also in their endurance and retention characteristics [15].

In contrast to other reactive metals in manganites-based RRAM devices, the W electrodes have been used very rarely in previous studies [11,18,19]. Nonetheless, Ignative et al. obtained excellent pulse endurance in PCMO-based devices by using W tips [18]. In addition to the endurance of the memory devices, the yield and reliability of the devices were improved by using a W TE along with thin films of barium–strontium titanate [(Ba, Sr)TiO_3] [20]. In addition, W has traditionally been used as an electrode material since it is compatible with CMOS-integrated circuits. Hence, it is expected that the W/PCMO interface can contribute to improving the reliability of nano-scale memory devices.

In this work, we have investigated the RS characteristics of a Pt/PCMO/W structure with the aim of elucidating the RS mechanism and, more importantly, of assessing its suitability for use in nano-scale memory devices. These devices show reproducible and stable RS behavior at a relatively low programming voltage (±1.5 V), while the resistance change was more than two orders of magnitude. On the basis of our experimental results, we suggest that the switching properties in the Pt/PCMO/W devices are interpreted by the oxidation and reduction of a WO_x layer at the

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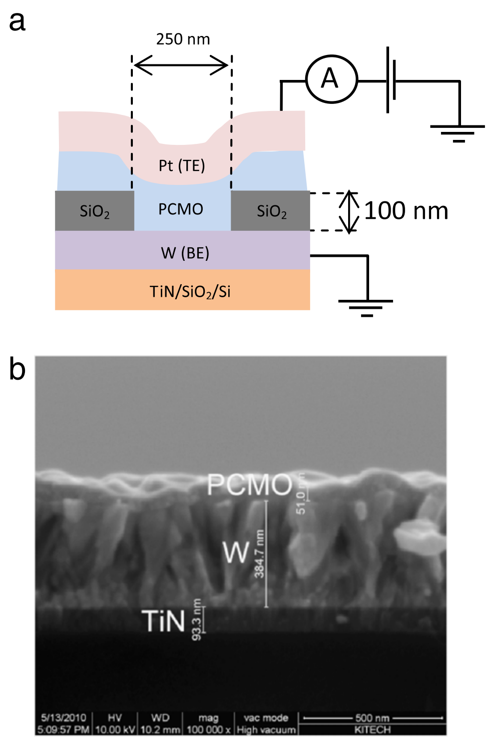

Fig. 1. (Color online) (a) Schematic illustration of the nano-scale Pt/PCMO/W memory devices with Φ250 nm via-holes structure and the measuring conditions. (b) Cross-sectional SEM image for the film grown at 650 °C for 5 min.

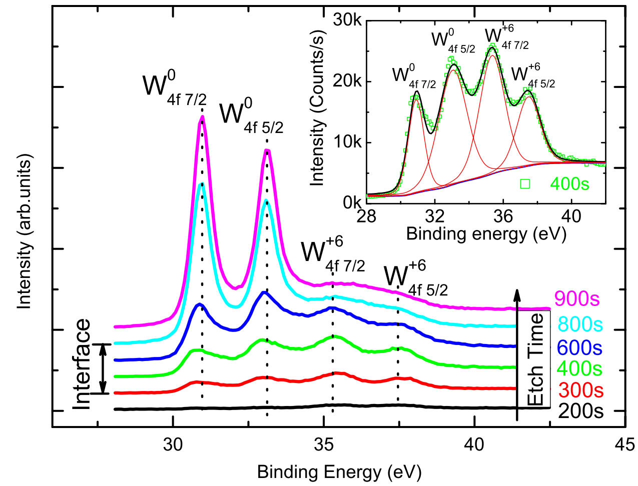

Fig. 2. (Color online) XPS spectra of W element of the PCMO/W interface. The inset shows the fitting results of W spectra at etch time of 400 s.

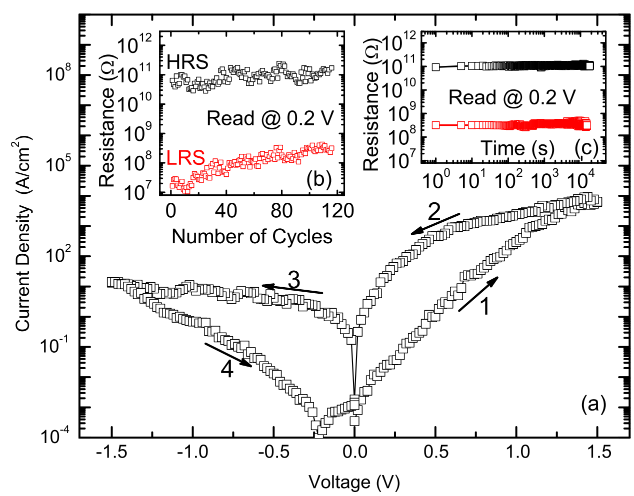

Fig. 3. (Color online) Resistive switching characteristics of nano-scale Pt/PCMO/W memory devices measured at room temperature. (a) Typical J–V curves, (b) endurance, and (c) retention performance.

interface of PCMO and W BE, and the low programming voltage is ascribed to the thermal-assisted RS and the unique properties of W metal and its oxides.

2. Experiments

First, a W BE was deposited with a thickness of 400 nm by chemical vapor deposition (CVD) on $TiN/SiO_2/Si$ substrates. Subsequently, a 100 nm-thick layer of SiO_2 was deposited on the W BE by plasma-enhanced chemical vapor deposition (PECVD). The next step consisted of Φ250 nm hole patterning by lithography and SiO_2 etching with a photo-resist mask. Polycrystalline PCMO films were deposited on the substrates with via holes by pulsed laser deposition (PLD) using a ceramic PCMO target. During the deposition process, the substrate temperature and working pressure of O_2 were kept at 650 °C and 10 mTorr, respectively. In order to decrease the oxidation of the W BE during deposition, an oxygen-deficient PCMO layer with a thickness of ∼10 nm was deposited at 3.3×10^{-9} Torr by means of a cryo pump. Lastly, a Pt TE with a thickness of 100 nm was deposited at room temperature (RT) by magnetron sputtering, followed by a lift-off process.

The electrical characteristics of the final Pt/PCMO/W structure for memory devices were evaluated using an Agilent 4155C semiconductor parameter analyzer. Fig. 1(a) shows the schematic structure of the nano-scale Pt/PCMO/W memory device and the measuring conditions. A positive bias was defined as a flow of current from the TE to the BE. Fig. 1(b) presents a cross-sectional SEM image of a PCMO thin film grown at 650 °C for 5 min. The PCMO layers had thicknesses of approximately 50 nm. All measurements were performed at room temperature.

3. Results and discussion

It is known that the metal oxides interface between a chemically reactive metal (M = Al, Ti, Ta, or Sm) and manganites plays an important role in RS [9–17]. To clarify the interface scenario, the chemical states of PCMO/W interfaces have been measured by the X-ray photoelectron spectroscopy (XPS) depth profile technique. Fig. 2 presents the typical W spectra at different etch times from 200 to 900 s. The depth level of 200 s indicates the maximum W diffusion location due to the stable W spectra appearing in the following levels. With further increasing the etch time, the number of W peaks changes from 4 to 2. The peaks of W4f can be fitted by four peaks: 30.9 eV ($W^0_{4f7/2}$), 33.1 eV ($W^0_{4f5/2}$), 35.3 eV ($W^{6+}_{4f7/2}$), 37.5 eV ($W^{6+}_{4f5/2}$), as shown in the inset of Fig. 2. The interlayer WO_x layer might be caused by the oxidation of W during the PCMO deposition or by the interdiffusion between the PCMO and W BE layers. The interfacial structure is responsible for switching properties as described below.

Fig. 3(a) shows typical current density–voltage (J–V) curves for the nano-scale Pt/PCMO/W memory devices. The voltage bias was scanned as follows: $0 \rightarrow +V_{max} \rightarrow 0 \rightarrow -V_{max} \rightarrow 0$ (indicated by arrows). Unlike traditional reactive metal/PCMO devices [7,9,10,13,16], the initial state of the Pt/PCMO/W memory cells exhibited a comparatively high resistance due to the existence of an interlayer WO_x layer; furthermore, no forming process was required to induce RS. RS from a high-resistance state (HRS) to a low-resistance state (LRS) is achieved by the application of a positive voltage. By sweeping the voltage to a negative value, an