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Gate-controlled transport in GaN nanowire devices with high-k Si_3N_4 gate dielectrics

Jae-Woong Lee, Moon-Ho Ham, Jae-Min Myoung*

Information and Electronic Materials Research Laboratory, Department of Materials Science and Engineering, Yonsei University, 134 Shinchon-Dong, Seoul 120-749, Republic of Korea

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Abstract

The high dielectric constant layer, Si_3N_4, was applied to the GaN nanowire devices. Single-crystalline wurtzite GaN nanowires prepared by the vapor–liquid–solid method were utilized to fabricate GaN nanowire field-effect transistor structures with Si_3N_4 and SiO_2 dielectric layers in order to investigate the effect of a high-k dielectric layer on the electrical characteristics of the GaN nanowires. By applying high-k gate dielectrics to GaN nanowire devices, higher drain current, lower subthreshold swing, and threshold voltage shift were obtained in spite of the slight degradation of the channel mobility due to the surface phonon scattering and the electrical scattering at fixed charges and trapped charges.

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1. Introduction

Further scale-down and higher integration of semiconductor devices are the main issues of metal-oxide-semiconductor field-effect transistors (MOSFETs). To respond to the continual size reduction, the application of one-dimensional nanostructures such as nanowires, nanotubes, and nanobelts has been proposed. Among several III–V compound semiconductors, GaN possesses good thermal stability, room-temperature ferromagnetism, chemical inertness, and a direct wide bandgap of 3.4 eV at room temperature [1–3]. Because of its superior properties, it has been extensively investigated for use in short-wavelength optoelectronic devices [4,5], high-power and high-temperature electronic devices [6], and room-temperature operating spintronic devices [7]. Meanwhile, nanostructures have unique physical properties such as high crystalline quality, large surface area, and a quantum confinement effect. Therefore, GaN nanowires have been considered as a building block for nanoelectronics, nanophotonics, and nanospintronics [8,9].

The continual scaling of a gate oxide brings about a higher leakage current caused by tunneling through a less than 1 nm-thick SiO_2 dielectric layer. In order to solve this problem, high-k dielectrics have been studied because they have the desirable effective oxide thickness (EOT) referred to pure SiO_2 as a physically much thicker film, thus avoiding the problems of tunneling [10,11]. Among various high-k gate dielectrics, Si_3N_4 is an attractive candidate due to its relatively high dielectric constant ε_r (=7.5), fine surface morphology, and low interface trap and bulk charge densities. Moreover, the Si_3N_4 effectively suppresses boron penetration in p-MOSFETs [12].

In this paper, single crystalline GaN nanowire devices configured as an FET structure were fabricated with a high-k Si_3N_4 dielectric layer. From the comparison of their electrical properties with GaN nanowire devices fabricated with an SiO_2 dielectric layer as a reference, the effect of a high-k dielectric layer on the GaN nanowire devices was investigated.

2. Experimental

The GaN nanowires were synthesized using the vapor–liquid–solid (VLS) growth mechanism. GaN powders (99.99%) were thermally evaporated in a horizontal tube furnace under

* Corresponding author. Tel.: +82 2 2123 2843; fax: +82 2 365 2680.
E-mail address: jmmyoung@yonsei.ac.kr (J.-M. Myoung).

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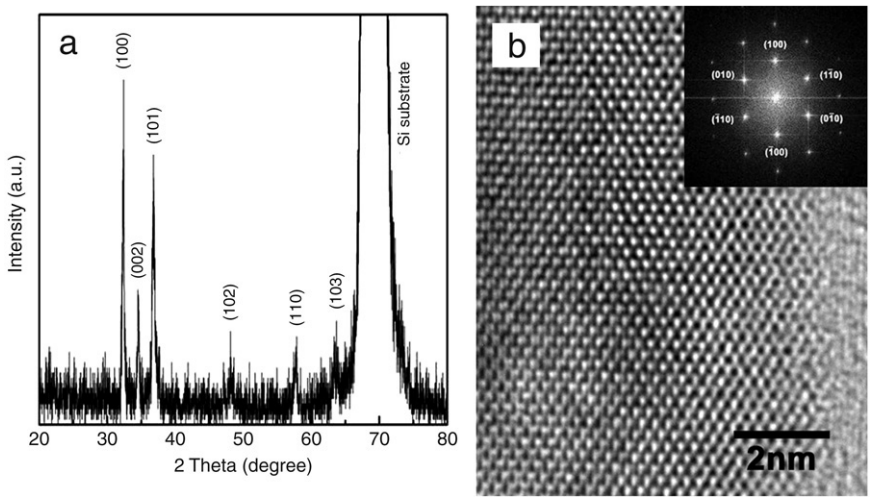

Fig. 1. (a) Representative XRD pattern for the GaN nanowires. (b) Representative HRTEM image and SAED pattern of a single GaN nanowire whose growth direction is along [100].

high-purity NH_3 (99.999%) gas flow with a rate of 35 sccm at 600 mTorr. The temperature was raised to 1100 °C at a rate of 36 °C/min and was maintained for 30 min. Si(100) substrates coated with 5 nm-thick Ni thin films were prepared, and rapid thermal annealing was subsequently performed at 900 °C for 3 min to make Ni islands which increase the density of nanowires and enhance the uniformity of nanowire shape. Then, the substrates were located at the downstream of the furnace with a separation of about 90 mm from the sources, i.e. in the colder zone near the venting outlet. After the synthesis process, GaN nanowires with lengths up to 8 μm and diameters from 30 to 60 nm were obtained on the substrates. The crystal structure of the synthesized nanowires was analyzed using x-ray diffraction (XRD) and high-resolution transmission electron microscopy (HRTEM). In order to fabricate the FET structure, GaN nanowires were released from the substrates by sonication in isopropyl alcohol and subsequently transferred to a degenerately doped p-type Si substrate capped with a thermally grown 300 nm-thick SiO_2 layer and a 300 nm-thick Si_3N_4 layer, where underlying Si was used as a back gate. The Si_3N_4 layer as a high-k dielectric was deposited using SiH_4 and NH_3 gases at a substrate temperature of 320 °C by plasma-enhanced chemical vapor deposition (PECVD). The position of the randomly distributed nanowires on the substrate was confirmed using a field-emission scanning electron microscope (FESEM). Then, the source and drain electrodes were defined on the ends of the nanowires using electron beam lithography which was followed by sputtering of Ti/Au (50/200 nm). Finally, rapid thermal annealing was performed at 600 °C for 60 s in an N_2 atmosphere to improve electrical contact. In order to confirm the reproducibility of the devices, we have fabricated at least 10 GaN nanowire devices with each gate dielectric. The electrical characteristics of the GaN nanowire devices with SiO_2 and Si_3N_4 gate dielectrics were investigated by using the HP-4145B semiconductor parameter analyzer.

3. Results and discussion

The GaN nanowires were characterized with Cu Kα radiation by an x-ray diffractometer. In Fig. 1(a), the XRD spectrum shows peaks of (100), (002), (101), (102), (110), and (103), indicating that the GaN nanowires have a hexagonal wurtzite structure with lattice parameters of $a = 3.189$ Å and $c = 5.185$ Å.

In order to identify the crystal structure of the GaN nanowires in detail, HRTEM analysis was performed. Fig. 1(b) shows a representative HRTEM image of a single nanowire along with the corresponding selected area electron diffraction (SAED) pattern. It shows that the as-synthesized GaN nanowires have no dislocations or stacking faults, revealing that the nanowires are highly crystalline. The lattice spacing of the GaN nanowires is estimated to be 0.275 nm from the clear lattice fringes of the HRTEM image. The HRTEM image and SAED pattern demonstrate that the nanowires have a single-crystalline GaN wurtzite structure with the growth direction along [100], consistent with XRD measurement.

The GaN nanowire devices with different gate dielectrics were fabricated in order to investigate the influence of the high-k dielectric on the electrical characteristics of devices. The SiO_2 layer was used as a reference gate dielectric. In the GaN nanowire devices with the SiO_2 gate dielectric, the channel current versus drain-source voltage (I_{ds}–V_{ds}) characteristics at different gate voltages (V_g) and transfer characteristics (I_{ds}–V_g) were measured at room temperature, and the results are shown in Fig. 2(a) and (b), respectively.

Fig. 2(a) showed that the conductance of the nanowires increased with increasing V_g, indicating that the GaN nanowires are n-type. Based on previous studies [13,14], this n-type behavior of undoped GaN nanowires is due to nitrogen vacancies, trace oxygen impurities, and surface defects coming from the large surface area of nanowires, which act as the scattering centers in the channel. As shown in Fig. 2(b), from the transfer curves obtained with full sweep, a clear hysteresis was observed. It is presumably due to trap charges arising from