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Evaluation of Cu(V) self-forming barrier for Cu metallization

Fei Cao*, Gao-hui Wu, Long-tao Jiang

School of Materials Science and Engineering, Harbin Institute of Technology, 150001 Harbin, China

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ABSTRACT

The properties of Cu(V) alloy films were investigated to evaluate its potential use as self-forming diffusion barrier in copper metallization. Cu(V) alloy films were deposited on SiO_2/Si substrates by magnetron sputtering. Cu(V)/SiO_2/Si systems were subsequently annealed at various temperatures and analyzed by four-point probe measurement (FPP), X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM). After annealed at 500 °C, the resistivity of the Cu(V) films reduced to 3.1 μΩ cm, there is no obvious increase in resistivity. XRD suggest that Cu alloy film has preferential (111) crystal orientation and no extra peak corresponding to Cu and Si even after annealed at 500 °C. According to TEM results, a self-formed thin layer with the thickness of about 8 nm is observed at the interface between Cu alloy and the SiO_2/Si substrate in the sample annealed at400 °C. As XPS results, after annealed at 400 °C and 500 °C, V atoms are observed at the surface of the Cu(V) films and the interface of the Cu(V) and SiO_2/Si. The formation of the self-formed thin layer is probably due to the separation of V at the interface. The sharp declines of the Cu and Si concentrations at the interface indicate a lack of inter-diffusion between Cu and SiO_2/Si. Adding small amounts of V to Cu film can improve the barrier performance and thermal stability compared with pure Cu contact systems.

1. Introduction

Copper has been extensively accepted as an advanced interconnect material in ultra-large-scale integrated (ULSI) devices because of its lower resistivity and batter electromigration resistance [1,2]. However, Cu inter-diffuses easily with dielectric materials such as SiO_2 even at low annealing temperature which results in the deterioration of the device performance. So it is necessary to insert a diffusion barrier to prevent the inter-diffusion [3–8]. The presence of the barrier layer increases the effective resistivity of the interconnect systems, so the thickness of the barrier layer should be controlled as thin as possible. However, the formation of the thin diffusion barrier with conventional technique has become difficult as the desired barrier thickness is only 5 nm respectively for the technology node reduced to 45 nm [9]. A self-forming barrier process has been proposed. In this process, Cu thin film alloyed with a strong oxide former such as Al and Zr is deposited directly on a dielectric layer such as SiO_2, then followed by heat treatment. The alloying element is supposed to migrate to the interface and form an ultra-thin layer as the diffusion barrier [10–16]. Self-forming barrier layers have been considered as an alternative barrier structure to the conventional Ta/TaN barriers. V and Ta are in the same group in the periodic table and V is a refractory metal that does not react with Cu[1]. The impurity diffusivity of V is 2.48 cm^2/s that is higher than the self-diffusion of Cu (0.78 cm^2/s) [17]. It is expected that V atoms may diffuse out of the Cu alloy film to the surface of the film and the interface of the film and SiO_2/Si after annealed. Our present work investigated the possibility of the self-forming barrier using Cu(V) thin films deposited directly on SiO_2/Si substrates. Based on the results of the samples before and after annealing at 500 °C, we can get the conclusion that Cu(V) alloy would be an attractive material for barrier-free Cu metallization.

2. Experiment

N-Type silicon wafers covered with 80 nm-thick thermal oxide layers were used as substrates(SiO_2/Si). Prior to alloy films deposition, the substrates were ultrasonically cleaned with acetone and isopropyl alcohol. The Cu(V) alloy films were deposited by magnetron sputtering system under an Ar plasma using a special made Cu(V) alloy target which contended 2 at% V. The deposition was performed at room temperature, the base pressure in the vacuum chamber was 1.0×10^{-4} Pa, and the working pressure was 0.5 Pa during sputtering with a fixed Ar flow rate of 20 sccm. The

* Corresponding author.
E-mail addresses: caofei1982@yahoo.com (F. Cao), wugh@hit.edu.cn (G.-h. Wu).

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sputtering power was kept at 90 W. After deposition, the Cu(V)/SiO_2/Si samples were vacuum-annealed at pressure of 1×10^{-3} Pa for an hour in 300–500 °C temperature range. Resistivity of the films was measured using the four-point probe method (FPP). Characterization of phase composition and crystallographic structure of the films were identified using X-ray diffraction (XRD, PANalytical X'Pert Pro) operated at 40 KV and 40 mA, with Cu K_ radiation. The depth composition profiles of the Cu(V)/SiO_2/Si and Cu/SiO_2/Si systems were obtained at room temperature using X-ray photoelectron spectrometer (XPS) (Thermo Fisher Scientific, USA) with monochromatic Al-Kα radiation (1486.6 eV). XPS measurement was carried out on the surface of the films after sputtering by Ar-ion, where the beam energy were used to be 1 keV. Cross-sectional images of the systems were observed using transmission electron microscope (TEM, Japan Electron Optics Laboratory Co.,LTD, JEM 2100). The acceleration voltage of TEM was 200 kV. The TEM samples (Φ3 mm) were prepared using an Ion Polishing System (GATAN 691).

3. Results and discussion

Fig. 1 plots the resistivity of Cu(V) alloy films and pure Cu films as a function of annealing temperatures ranging from 300 to 500 °C. The resistivity of as-deposited Cu(V) film is 8.1 μΩ cm which is higher than that of pure Cu film (4 μΩ cm). It is because that the Cu alloy films have fine grains and there are many incorporated additives which will increase resistivity of the Cu alloy [18]. Also, the resistivity of both of the films are higher when compared with that of their bulk material. It is because the high defect density and large surface-to-volume ratio of thin films will increase the resistivity. When the annealed temperature raising to 300 °C, the resistivity of Cu(V) and pure Cu films decreases slightly, the reduction is more obvious for Cu (V) film compared with pure Cu film. The significant decrease in resistivity of Cu(V) films may be attributed to the reduction of defects and the out-diffusion of alloy content from the film to the surface and the interface of the alloy film and the SiO_2/Si substrate. As the annealing temperature increases further, the resistivity of the pure Cu film rises slightly after 400 °C annealing, and rises significantly after annealing at 500 °C. The sharp increase in resistivity may be attributed to the formation of new material (as Cu_3Si) with higher resistivity, it will be proved by the XRD results in which copper silicide phase can be detected when annealing temperature raising to 400 °C for Cu/SiO_2/Si sample. But for Cu(V)/SiO_2/Si sample, the resistivity of Cu(V) films continue to decrease even when the temperature raising, it can reach the lowest value of 3.1 μΩ cm when annealed at 500 °C there is no obvious increase in resistivity even after annealing at 500 °C. This suggests that a small amount of V added to Cu can improve the thermal stability of resistivity for Cu interconnection system.

Fig. 2 shows the XRD patterns of Cu/SiO_2/Si and Cu(V)/SiO_2/Si samples before and after annealed at different temperature. Diffraction peaks that correspond to the (111) lattice planes of Cu crystal structure are present in the as-deposited and annealed films for both samples. With the increase of the annealing temperatures, the Cu peaks become sharper which attributed to grain growth in the copper layer. Diffraction peaks corresponding to V precipitates are not observed due to the small amount of alloying element used. After annealed at 400 °C for Cu/SiO_2/Si samples as shown in Fig. 2(a), we can detect a small new peak as Cu_3Si, this Cu_3Si with high resistivity may be caused by the reaction of Cu and the SiO_2/Si substrate. When annealing temperature raising to 500 °C, the Cu_3Si peak increases, which is in accordance with the results of resistivity. For Cu(V)/SiO_2/Si samples, as shown in Fig. 2(b), there is no peak corresponding to compound consisting of Cu and Si even when the annealing temperature raising to 500 °C.It indicates that there is no

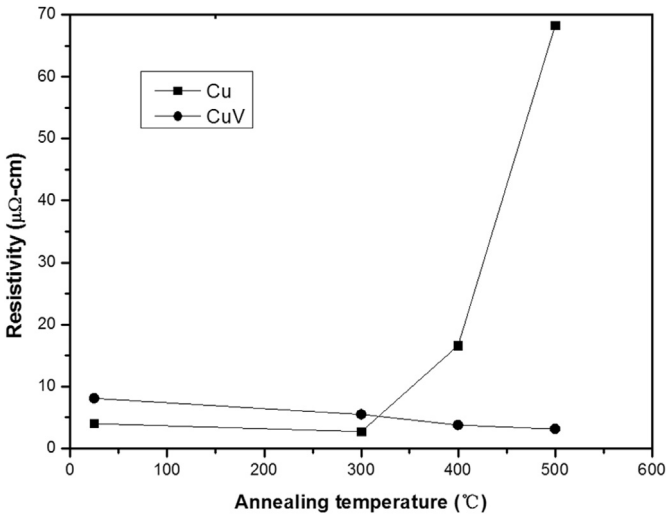

Fig. 1. The resistivity of the Cu(V) and Cu films as a function of annealing temperatures.

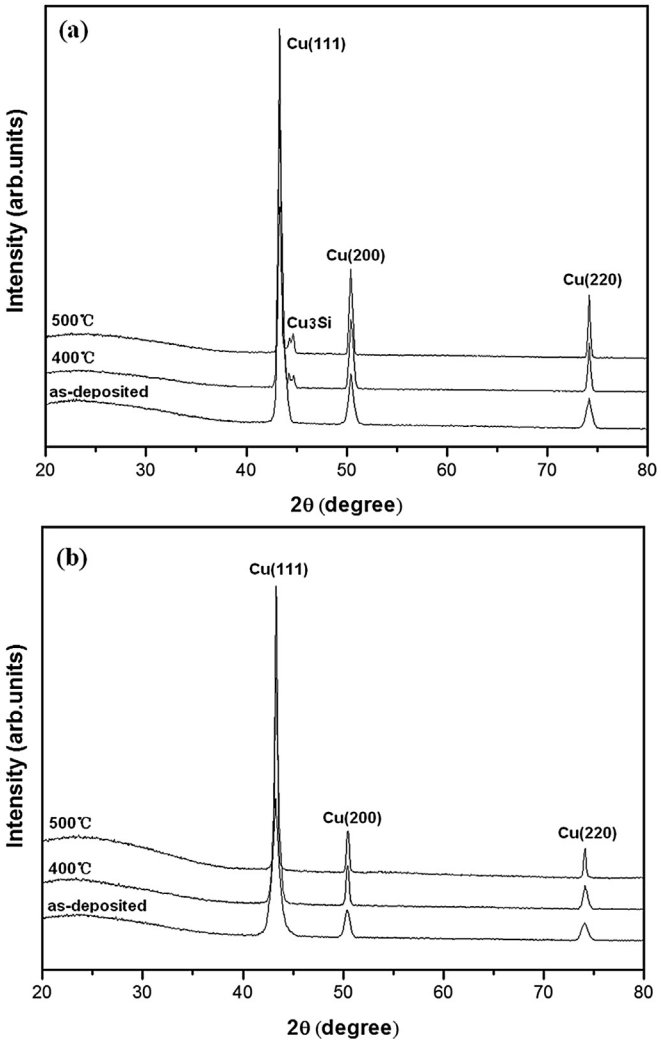

Fig. 2. The XRD patterns of samples before and after annealing. (a) Cu/SiO_2/Si; (b) Cu(V)/SiO_2/Si.