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Effects of interface states and series resistance on electrical properties of Al/nanostructure CdO/p-GaAs diode

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ABSTRACT

The nanostructure CdO thin film was grown on p-GaAs substrate by the sol–gel method. Electrical characterization of Al/CdO/p-GaAs diode was performed using current–voltage and capacitance–conductance–voltage measurements. The ideality factor and barrier height values of the diode were obtained to be 2.29 and 0.62 eV, respectively. The energy distribution profiles of interface states were determined by means of Hill–Coleman method. The obtained results revealed that the series resistance and interface states have an important effect on electrical characteristics of Al/CdO/p-GaAs diode.

1. Introduction

Metal-thin interfacial insulator layer-semiconductor devices have been extensively used in modern electronic applications such as, microwave diodes, field-effect transistors (FETs), solar cells and photodetectors. Most of the studies have been done on characterization and improvement of the interface properties of the diodes [1–14]. It is well known that interfacial oxide layer has considerable effects on device performance in terms of reliability and stability and the choice of interfacial layer is also important, because silicon dioxide (SiO_2) cannot completely passivate the active dangling bonds at the semiconductor surface in metal–semiconductor structures. Therefore, use of the non-traditional materials such as Si_3N_4 [6], ZnO [7], SnO_2 [8], TiO_2 [9], PbS [10] and doped polymers [11] will be an interesting subject for surface passivation.

On the other hand, transparent conductive oxide thin films (TCO) such as zinc oxide, indium–tin oxide, and cadmium oxide (CdO) have been extensively investigated because of their use in semiconductor optoelectronic device technology [15,16]. Among these, CdO has received a considerable attention for photovoltaic applications on account of its low electrical resistivity and high transparency in the visible range of solar spectrum [16–18]. Moreover, the higher mobility values ($\mu = 216\ cm^2\ V^{-1}\ s^{-1}$) [13] were obtained for CdO films. High mobility value is a necessity for high-conductivity TCO materials, especially when low free-carrier absorbance is preferred. Undoped and doped CdO thin films can be deposited by several physical and chemical deposition techniques such as sol–gel [16,18–21], pulsed laser deposition [17], DC magnetron sputtering [22], radio-frequency (rf) sputtering [23], spray pyrolysis [24], chemical vapor deposition [25] and chemical bath deposition [26], and successive ionic layer adsorption and reaction (SILAR) methods [27]. Among them, sol–gel method, which is a low cost and easily scaleable method, offers several advantages; such as composition control, homogeneity, purity, simplicity and also it is possible to cover large areas with irregular geometry [18–21].

Some studies have been done on electrical characterization of CdO Schottky devices or heterojunctions fabricated by different methods [18,27,28]. Saglam et al. [27] have prepared Cd/CdO/n–Si/Au–Sb sandwich structure using SILAR method and Yakuphanoglu [18] has synthesized the nanocluster CdO film by sol–gel method and has investigated the structural, electrical and photovoltaic properties of the device. Also, Farag et al. [28] have deposited undoped and doped CdO films on p-Si by sol–gel method, and have presented the morphological properties of the diodes. It is well known that electrical characteristics of Schottky barrier diodes (SBDs) are often affected by various factors; such as interface states, series resistance, and interfacial insulator layer. In presence of such an interfacial layer, the C–V and G/ω–V characteristics of MIS type SBDs deviate from the ideal behavior of MS diodes. The capacitance of a SBD in the idealized case is usually frequency independent, especially at high frequency limit. However, the situation is different especially at low frequencies due to the effects of

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interfacial layer, R_s and particularly distribution of N_{ss} localized at the interface between insulator and semiconductor layers. The interface state density can be considered as electronic states generated by unsaturated dangling bonds of the surface atoms. Furthermore, these states can create a charge distribution at the interface or traps, affecting the value of capture cross sections of the traps [4,5]. Some studies have explained the presence of anomalous peak in the forward bias *C–V* characteristics and the origin of such peak has been attributed to interface state density by Ho et al. [29]. Also, Altındal et al. [11] and Werner et al. [30] have explained that the observed peak in *C–V* plot at forward bias is due to series resistance effect. However, Wu and Yang [31] have showed that the peaks in *C–V* plots are arised from interface state density rather than series resistance. On the other hand, Chattopadhyay et al. [32] theoretically have showed that presence of the peak in CV- plots and its position depend on various parameters such as R_s, N_{ss}, doping concentration and thickness of interfacial insulator layer.

There are several suggested methods to determine R_s of a Schottky barrier diode, however, they suffer from a limitation of the applicability [5,33–35]. Among them, the most important and practical one is the conductance technique proposed by Nicollian and Brews [5]. According to this method, *C–V* and G/ω–*V* measurements under forward and reverse biases yield significant information about interface state density and series resistance.

The aim of present study is to investigate the effects of interface state density and series resistance on the electrical characteristics of Al/CdO/p-GaAs diode. For determination of the interface states of the diode, we used the conductance method. The frequency dependence of interface state density was obtained from *C–V–f* and G/ω–*V–f* characteristics of the diode.

2. Experimental details

The substrate used in this study is p-GaAs (100)-doped with zinc. The substrate was sequentially cleaned with trichloroethylene, acetone, methanol and then rinsed in de-ionized water of 18 MΩ and dried with high purity N_2. The native oxide on the surface of semiconductor was etched in sequence with acid solutions (H_2SO_4:H_2O_2:-H_2O = 3:1:1) for 60 s, and (HCl:H_2O = 1:1) for another 60 s. Again, it was rinsed in de-ionized water and dried with high purity N_2. Ohmic contact on the back of p-type GaAs wafer was formed by thermal evaporation of indium metal using a VAKSIS thermal evaporation system under 2×10^{-5} Torr and the prepared contact was thermally treated at 370 °C for 5 min in N_2 atmosphere.

CdO film was synthesized by the sol–gel method. The used source materials are cadmium acetate, deionized water and monoethanolamine. Equal concentrations of monoethanolamine and cadmium acetate were used. The precursor solution was stirred with a magnetic stirrer for 2 h at 60 °C, until a clear and homogeneous solution was obtained. Thin film of CdO was coated on the clean front surface of the GaAs substrate using a spin coater at 1000 rpm for 1 min. After a solid thin film on the substrate was formed, the film was annealed at 470 °C in a furnace. Aluminium contacts of 100 nm thickness were formed on CdO film by thermal evaporation. The diode contact area of Al/CdO/p-GaAs diode was found to be 3.14×10^{-2} cm^2. The electrical characterization of the diode was done using a KEITHLEY 4200 semiconductor characterization system. The structural properties of CdO film were investigated using a PARK system XE100E atomic force microscopy (AFM).

3. Results and discussion

Fig. 1 shows AFM images of CdO film. As seen in Fig. 1, the CdO film is formed from the nanoparticles, suggesting that the CdO film has the nanostructure. It is expected that the nanostructure of CdO will affect the performance of the studied diode.

3.1. I–V characteristics of Al/CdO/p-GaAs diode

The current–voltage characteristics of Al/CdO/p-GaAs diode are shown in Fig. 2. As seen in Fig. 2, at lower voltages, the current of the diode changes exponentially with the applied voltage. This suggests that the current–voltage characteristics of the studied sample can be analyzed by thermionic emission (TE) theory. The charge

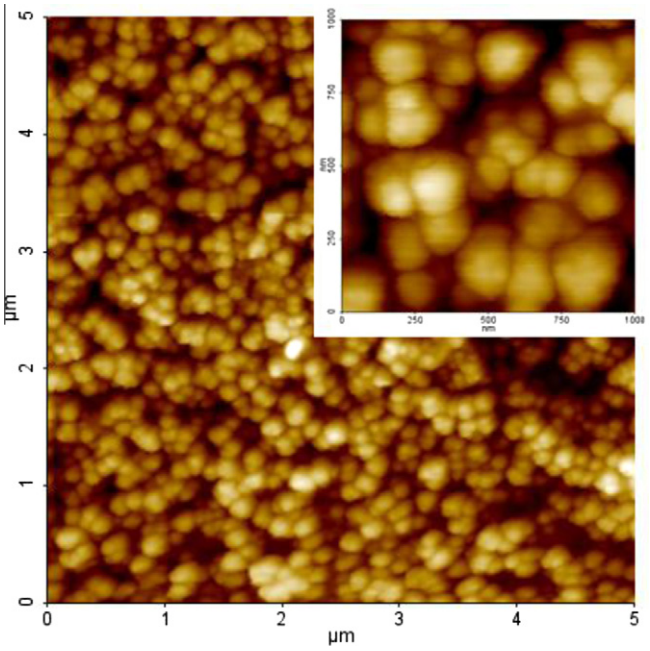

Fig. 1. AFM image of CdO film deposited onto GaAs substrate.

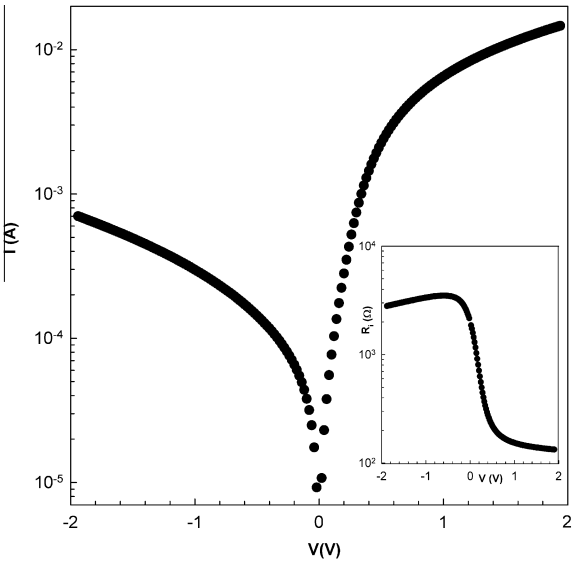

Fig. 2. The semi-logarithmic *I–V* plot of Al/CdO/p-GaAs SBD at room temperature. Inset shows R_i–*V* plot.

transport mechanism of a diode having series resistance can be analyzed by the following equation [1,2],

$$I = I_o \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{kT}\right)\right] \quad (1)$$

where I_o is the reverse-saturation current given by,

$$I_o = AA^*T^2 \exp\left(\frac{-q\Phi_{Bo}}{kT}\right) \quad (2)$$

where Φ_{Bo} is the zero-bias barrier height, A is the diode contact area, A^* is the Richardson constant (79.2 A/cm^{2}K^2 for p-type GaAs) [36], q is the electronic charge, k is the Boltzmann constant, T is the absolute temperature and n is the ideality factor.

Fig. 2 shows a linear behavior in voltage range of $0.06 \leqslant V \leqslant 0.40$ V. However, at sufficiently higher applied voltages, there