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# Anatomizing the Impact of High Dielectric Gate Materials on the Charge Transport in Graphene Field Effect Transistors

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**Abstract**

We have investigated the impact of different dielectric materials as gate dielectric in ZAZ structures for a particular width and central region using density functional theory (DFT) with self–consistent calculations within the framework of Non-Equilibrium Green Function (NEGF) by using Krylov methods as self-energy calculator in ATK 13.8.0. The length of the channel separation and width is taken to be 4 and 6 respectively. In this case we only varied the left electrode voltage and kept right electrode voltage to be zero so that net effect of the $V_{DS}$ can be observed. The $V_{DS}$ is varied by keeping all the parameters constant and then the graphs are plotted for IV curves, differential conductance (dI/dV). The distinct changes in conductance and I-V curves reported as the material of gate dielectric was varied for low-κ dielectrics like 2 ,4, 8 as well as high-κ dielectrics like 18,20,25 etc. at different bias voltages from -2V to 2 V with steps of 0.5 V. From the simulated results we observed that the maximum conductance reported for high dielectrics 25 ($CeO_2$) is in the range of $10^{-5}$ siemens whereas the maximum conductance reported for low dielectrics 4($SiO_2$ ) is in the range $10^{-6}$ siemens through Z-A-Z (GFET) structures for positive bias voltages.


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*Keywords:* Charge Transport, GFET, High-κ Dielectrics, Density Functional Theory (DFT), NEGF, GGA, Gate voltage, Channel Length, ATK - 13.8.0 (VNL).

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## 1. Introduction

Since the report of the preparation of graphene by Novoselov et al. in 2004, there has been an enormous and rapid growth in interest to the semiconductor -industry because this material is compatible with planar technology [1-4]. Graphene has attracted intensive interest due to its fundamental properties and potential applications in future electronic devices [5-8]. One of the most important properties of graphene is a strong electric field effect which leads to an electrostatically tunable carrier density in the range of n < 1014 cm-2. Together with high carrier mobilities for both electrons and holes[9-10] (as high as 104 cm2 /Vs at room temperature), this attracts a lot of attention to graphene as a possible material for a future high-speed field effect transistor (FET)[11].

The graphene nanoribbon (GNR) based devices and even integrated circuits can be fabricated by a single process of patterning a graphene sheet. The Field Effect Transistor (FET), which is the most building block of a majority of the modern ICs, has undergone many phases of development since its invention. The Graphene Nanoribbons (GNRs) with finite width are important components of graphene nano-structures. Electrical properties of GNRs are much more sensitive to the orientation and width which offers great possibilities for their electronic devices applications. When the width across layer, Channel length, gate voltage, gate dielectric material and electron temperature is varied at different bias voltages between two electrodes, the GNRs shows different charge transport mechanisms[12].

By the time the FET was invented Silicon had already replaced Germanium as a result of the excellent properties of $SiO_2$. The Metal Oxide Semiconductor (MOS) technology saw a transition from PMOS to NMOS to CMOS as a result of development in fabrication. These developments were aimed at achieving mobility enhancements and reduction in power dissipation.

But as the thickness of SiO2gate dielectric films used in CMOS devises is reduced towards 1 nm, the leakage current level becomes unacceptable [13-15].This leakage arises from quantum effects. At 1 nm, the quantum nature of particles starts to play a big role. Extensive efforts have been focused on finding alternative gate dielectrics for future technologies to overcome leakage problems [16-17]. The goal was to identify a gate dielectric material as a replacement for SiO2and also to demonstrate transistor prototypes that leaks less while at the same time driving plenty of current across the transistor channel. We needed a gate insulator that was thick enough to keep electrons from tunneling through it and yet permeable enough to let the gate's electric field into channel so that it could turn on the transistor. Hence the material had to be physically thick but electrically thin.

Oxide materials with large dielectric constants have attracted much attention due to their potential use as gate dielectric in MOSFETs. Thicker equivalent oxide thickness, to reduce the leakage current of gate oxides, is obtained by introducing the high –k dielectrics in real application [18]. The dielectric constant (dielectric 'k') refers to a materials ability to concentrate an electric field. The k-value is related to how much a material can be polarized. When placed in an electric field, the charges in a dielectric's atoms or molecules will reorient themselves in the direction of the field. These internal charges are more responsive in high-k dielectrics than low-k ones. Having higher dielectric constant means the insulator can provide increased capacitance between two conducting plates i.e. storing more charge, for the same thickness of insulator. It can provide the same capacitance with a thicker insulator [19-20].

By connecting graphene nano-ribbons (GNRs) of different widths, graphene PN junctions or quantum dots can be formed. Apart from changing the width, patterning graphene nano-ribbions with different edge types (Z-A-Z or A-Z-A) is another way to form graphene electronic devices [21]. The graphene sheet serves as the FET channel and sits on the top of a stack of dielectric and conducting material. The graphene sheet, the dielectric and conducting material form a parallel plate capacitor with the conducting material acting as the gate (G). The graphene sheet is connected to conducting contacts at the edges which serves as a Source (S) and Drain (D).

A field effect transistor (FET) can be modeled simply by two metal-semiconductor interfaces. The potential applications for the model can be the perfect atomic interface, a feature that is difficult to achieve for the interconnection between nanotubes of different diameters and chirality and GNR based devices can be connected to the outside circuits exclusively via metallic GNRs where as it is difficult to find a robust method to make contact with molecular device .The extension of metal electrodes provided to make contact with the semiconducting GNRs so that an atomically smooth metal-semiconductor interface is maintained with minimum contact resistance [22].