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A Novel Architecture for Scan Cell in Low Power Test Circuitry

G. Rajesh Kumar[a,*], K. Babulu[b]

[a]*Research Scholar, JNTUK, India*
[b]*Professor, JNTUK, India*

Abstract

Over the past decade VLSI manufacturing industry flourishing very rapidly. Now a days hundreds and thousands of millions of transistors that are incorporated on a chip. As the circuit complexity increasing design for test circuitry also became more complex. These complex test circuitry heavily stressed to check the functionality of the CUT (Circuit under Test). Compared with normal functional mode, Power dissipation during test mode is much higher. Power dissipation during testing is more than twice compared with normal functional mode. Large Test data volume and High power consumption are the main problems in Design for Testability. This excessive power consumption is mainly due to switching of the scan cells. The technique proposed in this paper reduces switching activity in the scan cells there by the power consumption during testing can be reduced. In the proposed scan cell architecture some of the idle flip-flops are disabled during scanning using a control signal. By disabling idle flip-flops can be possible by an external control signal or with any internal signal. Excessive power consumption during testing may cause performance degradation and high system cost. These problems can be eliminated with the proposed scan cell architecture.

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Keywords: CUT(Circuit Under Test); Design for Testability; Scan cell; Test data; Switching activity; VLSI(Very Large Scale Integration)

1. Introduction

As per Moore's law the number of transistors that can be integrated is continuously growing and crossed millions of transistors. As the technology improving the circuit complex also increasing. In order to design such a complex circuits new design techniques should be adopted. Many design challenges are adopted for complex digital circuit

* Corresponding author. Tel.: +91-9989437902.
E-mail address: kavi.aeiou@gmail.com

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design. Low power design is the major design objective which is widely observed in communication and signal processing circuits. Now a days many digital systems working on battery power. Frequent charging of these portable devices may be burden for the users. Power source for charging those devices may not be available all the time. If those devices consume high amount of power frequent charging is required for them. Because of this high power consumption battery may be reduced. In order to overcome this problem now a days designers are concentrating more on low power design techniques. On the other hand power consumption during testing is much higher compared with normal he circuitry with the help of scan chains. In the scan chain the test vector is loaded serially bit by bit. While storing test vectors serially in the chain, bit by bit there are so many unwanted change states of the scan cells. Power consumption during testing may be measured with the switching activity of the scan cells. If these unwanted switching of scan cells are reduced power consumption in test mode also reduces.

Excessive power consumption during test mode is very much high compared with normal functional mode. There are so many techniques proposed for low power design during normal functional mode. C. Shi et al. (2004) stated that the power consumption during test mode is several times of normal functional mode. Sabaghian-Bidgoli et al. (2012) stated that Power dissipation in digital circuits during scan based test is generally much higher than that during functional operation. Now there was a need to develop low power test techniques. The main reason why the power consumption is high in test mode is, many test pattern generating circuits concentrate more on pattern minimization and low test time. These test patterns may cause high switching activity and results high power consumption during testing.

2. High Power Effects

Power dissipation in VLSI circuits is such an important issue when it comes with portable devices. Now a day's portable device market increasing rapidly. These portable electronic devices depends on battery power. In battery operated devices power consumption matters a lot. According to Moore's law the circuit complexity and functionality increasing rapidly. High complex circuits with heavy functionality demands high speed computations. As the VLSI technology is advancing the transistor size is decreasing. Scaling of transistors increases power consumption rapidly. While in the development of portable devices power consumption is the main criteria. Because it is very difficult to assemble huge battery packs inside a portable electronic device. Frequent recharging of the portable devices is also a big headache for the consumer. Industry demands more features for portable devices with low power consumption and with low cost. If the devices are attached with high performance battery packs, cost also increases. By considering all these effects low power consuming device development is greatly needed.

In the case of mobile phones consumer wants a smart mobile phone with lots of features. Mobile phone it should be sleek, slim and weight less. It should have high speed data transmission capability, high talk time and with many functionalities like camera, Bluetooth, NFC (Near Field Communication) etc. In order to fulfill all these demands these smart phones must be equipped with advanced processors. These advanced processors need high amount of power. When smart phone is used for multiple applications the peripheral devices that are assembled also more. In order to work with those peripheral devices complex integrated circuits are needed. These

Because of this high power consumption battery life may be reducing. Battery packed used for portable devices stressed heavily while testing such a high complex circuits. This effects the degradation of battery life. Another important issue with high power consumption is the temperature raise. If the raise is temperature raise above a threshold value the Integrated Circuit may damage in some of the circuits the circuit functionality may change with the effect for high temperatures above a threshold temperature. Next is the parameter that effected by high power consumption is yield loss. Due to high temperature traditional cooling techniques may not sufficient. Expensive cooling techniques may be used. They may increase the cost of the IC also the area occupied may affect the yield loss. Because of the excessive test power heat dissipated also high. In order to handle high temperature costly packaging is required. Plastic packaging is very much cheap compared to all other packaging techniques. But plastic packaging not able to withstand for high temperature. Traditionally used plastic packaging may not handle such a high temperature. Instead ceramic or any other packaging technique which can withstand at that high temperature can be used. Expensive packaging may lead to increase of chip cost. High temperature and current density may lead to circuit malfunctioning. Due to high temperature and current density caused by high switching activity in the testable electronic circuitry may lead to malfunctioning of the circuit under test.