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Drop failure modes of Sn−3.0Ag−0.5Cu solder joints in wafer level chip scale package

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Abstract: To reveal the drop failure modes of the wafer level chip scale packages (WLCSPs) with Sn−3.0Ag−0.5Cu solder joints, board level drop tests were performed according to the JEDEC standard. Six failure modes were identified, i.e., short FR-4 cracks and complete FR-4 cracks at the printing circuit board (PCB) side, split between redistribution layer (RDL) and Cu under bump metallization (UBM), RDL fracture, bulk cracks and partial bulk and intermetallic compound (IMC) cracks at the chip side. For the outmost solder joints, complete FR-4 cracks tended to occur, due to large deformation of PCB and low strength of FR-4 dielectric layer. The formation of complete FR-4 cracks largely absorbed the impact energy, resulting in the absence of other failure modes. For the inner solder joints, the absorption of impact energy by the short FR-4 cracks was limited, resulting in other failure modes at the chip side.

Key words: Sn−3.0Ag−0.5Cu; wafer level chip scale package; solder joint; drop failure mode

1 Introduction

The approaches of miniaturization, light weight, high speed, and multifunction will be never-ending for electronic devices, which definitely results in higher density and smaller dimension of electronic package. To meet these increasing requirements from both market and technique, great efforts have been implemented to develop advanced packaging technologies. With simplified process, high production efficiency, reduced cost and small footprint, wafer level chip scale package (WLCSP) has become one of the most attractive emerging package technologies, especially in portable consumer market [1,2].

In electronic packaging, solder alloys are still the most commonly used interconnection materials. Due to the serious environmental and public health concerns on Pb, lead-free solders have been developed to substitute the traditional Sn−Pb solders [3,4]. So far, Sn−Ag−Cu alloys, typically Sn−3.0Ag−0.5Cu (SAC305), have been proved to be the most popular lead-free solders [5−7]. Since portable consumer electronics are frequently shocked and dropped in service, crack and even fracture may occur in solder joints or package substrate, which seriously degrades the reliability of the products. Hence, drop failure modes and mechanisms of solder joints as well as package substrate are quite important for product design and manufacturing.

Many studies on the drop reliability of Sn−Ag−Cu solder joints have been carried out. LAI et al [8] pointed out that solder joints with a low Ag content and substrate pads with organic solderability preservative (OSP) surface finish (another was Ni/Au) both enhanced the drop resistance of the board-level test vehicle. Besides, the failure mode statistics indicated that most of fractures located on the package side for high Ag content solder joints while on the test board side for low Ag content ones. SUH et al [9] reported that Sn−4.0Ag−0.5Cu solder typically exhibited interfacial fracture during drop testing, while Sn−1.0Ag−0.5Cu solder exhibited considerable amount of cohesive failure through bulk solder. The effects of minor alloying elements, such as Ni, Ge, Zn, Pd, In, Co, and Fe, on the failure modes of Sn−Ag−Cu solders in terms of drop impact and thermal cycling have also been investigated [10−13].

The structure of a package also plays an important role in the drop reliability. TUMNE et al [14] found that

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smaller array size, pitch and package height showed better drop reliability. FAN et al [15] reported that for a copper post (or pillar) wafer level package, wafer level epoxy, which encapsulated copper pillars, served as a compliant layer for solder joint stress reduction under dynamic loading. An elasto-plastic model was applied on both solder bump and copper pad materials to simulate the drop performance of WLCSPs and a good accuracy was obtained [16].

Up to now, few studies focus on the board level drop performance of WLCSPs with Sn−3.0Ag−0.5Cu solder joints, which is significant for the design and reliability evaluation of portable consumer electronics. In the present work, board level drop tests were performed using WLCSPs with Sn−3.0Ag−0.5Cu solder joints and the failure modes were identified and discussed.

2 Experimental

WLCSP products with real chips were used as the board level drop test samples. No underfill was used for these WLCSP products. Figure 1(a) shows a WLCSP specimen with four chips mounted on the printing circuit board (PCB). The PCB consisted of nine copper trace layers with FR-4 as the dielectric layers. The dimensions of the chips were 5.33 mm × 4.89 mm × 0.31 mm and those of the PCB were 100 mm × 50 mm × 0.78 mm. Four positioning holes with a diameter of 3 mm were fabricated at the corners of the PCB to fix the samples on the drop tester with the chips facing down. The horizontal distance between the positioning holes was 97 mm and the vertical distance was 40 mm.

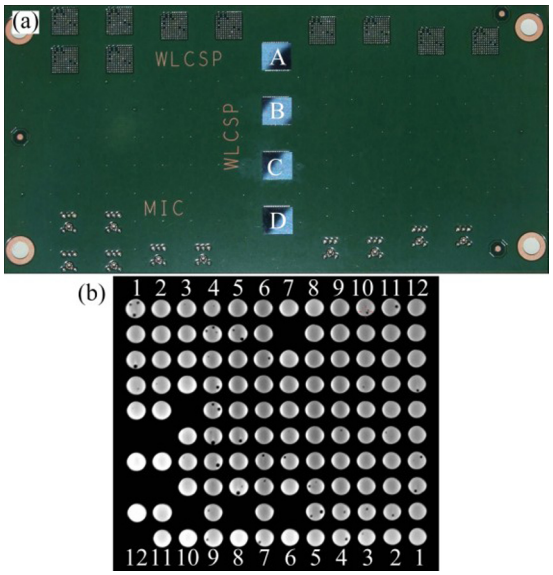

Fig. 1 WLCSP specimen (a) and X-ray image of chip (b)

The composition of the solder balls was Sn−3.0Ag−0.5Cu. The pads with 250 μm in diameter on the PCB side was OSP-Cu with non solder mask defined (NSMD) and the under bump metallizations (UBMs) on the chip side were Cu. The Cu UBMs were fabricated on redistribution layer (RDL). Figure 1(b) shows the X-ray image of one of the chips, clearly showing the configuration and array of the solder balls. Pores existed in some of the solder balls. The average diameter of the solder balls was 300 μm with a standoff height of 155 μm and a pitch of 400 μm.

Board level drop tests were carried out using CL20 impact test system according to the Joint Electron Devices Engineering Council (JEDEC) standard for drop testing—JESD22−B111 [17] and JESD22−B104C [18]. The drop tests were performed under a peak acceleration of 2900g (where g is 9.8 N/kg) and a pulse duration of 0.3 ms for 5000 drop times. After the drop tests, the WLCSPs were ground and polished for cross-sectional observation using a scanning electron microscope (SEM), in order to identify the failure modes. The deformation and stress in the WLCSPs were simulated using ABAQUS, in which the model was built using real geometric size and the properties such as density, elastic modulus, and Poisson's ratio were set using the values for real materials. The acceleration was applied on the centre of gravity of the test sample.

3 Results and discussion

3.1 Microstructure of as-soldered WLCSP

Figure 2 shows the cross-sectional SEM images of an as-soldered WLCSP sample. As shown in Fig. 2(a), intact interconnections were achieved between the chip

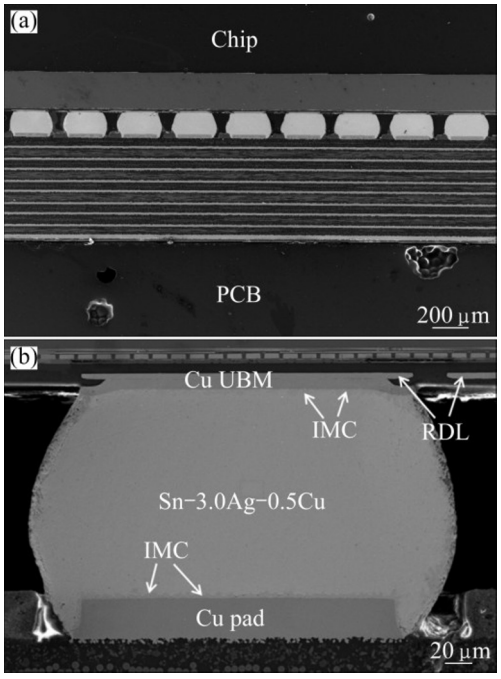

Fig. 2 Cross-sectional microstructures of as-soldered sample: (a) WLCSP; (b) Solder joint