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Formation of germanium (111) on graphene on insulator by rapid melting growth for novel germanium-on-insulator structure

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ABSTRACT

We demonstrate the crystallization of the microstrips of electrodeposited amorphous germanium (Ge) on graphene on insulator by rapid melting growth for the first time. Growth of single-crystalline Ge microstrips with (111) orientation was confirmed. The high level of compressive strain was found to be resulted from the intermixing of C atoms from multilayer graphene (MLG) and Ge. Probably the introduction of local C atom into Ge film enhances nucleation of Ge on MLG, which results in (111)-oriented Ge nuclei. Subsequent lateral growth enables crystallization of Ge with (111) orientation on the entire microstrip. The results also indicate that graphene is very useful to suppress the spontaneous nucleation in the melting Ge films and the lattice rotation or misorientation. This novel and innovative technique provides a breakthrough towards the realization of high quality Ge-on-insulator structures to facilitate the next-generation ultra-large-scale integrated circuits (ULSIs) with multifunctionalities.

1. Introduction

The performance of silicon ultra-large-scale integrated circuits (Si-ULSIs) has been enhanced over the last 30 years by increasing the number of transistors in accordance with Moore's law [1]. The scaling rule of the Si transistor has made it possible to enhance the performance of the ULSIs. However, the miniaturization of the transistors becomes increasingly difficult owing to the physical limitations, and the conventional scaling rule will not be enough to enhance the performance of the ULSIs. Recently, the concept of advanced heterogeneous integration on Si platform was proposed by Takagi et al. towards the realization of a so-called "More than Moore" technology [2]. They proposed new semiconductor materials with higher mobility than Si such as germanium (Ge) to be introduced on the Si platform in order to not only enhance the performance of MOS transistors [3] but also to facilitate the present ULSIs with various functionalities where these materials can be used to fabricate various kinds of functional devices, such as optical devices, photodetectors, and solar batteries. In order to fabricate electronic devices in Ge, it is necessary to electrically isolate the Ge and the Si substrate by insulator. Therefore, some breakthrough on growth technologies is strongly required to realize high quality Ge-on-insulator (GOI) structures.

Graphene is a two-dimensional hexagonal network of carbon atoms which is formed by making strong triangular σ-bonds of the sp^2 hybridized orbitals. This bonding structure is similar to the *c*-plane of a hexagonal crystalline structure and (111) plane of diamond structure. With this regard, the growth of (111) oriented Ge on graphene direction is feasible. It is well documented that graphene has a great potential for novel electronic devices to act as device channel, transparent electrode, sensing membrane and so forth, because of its extraordinary electrical, thermal, and mechanical properties, including a carrier mobility exceeding 10^4 cm^2/Vs and a thermal conductivity of 10^3 W/mK [4–8]. Therefore, with the excellent electrical and thermal characteristics of graphene layers, growing Ge nanostructures and thin films on graphene layers would enable this Ge/graphene/SiO_2/Si material system to be exploited in diverse sophisticated device applications.

It is well documented that the rapid melting growth (RMG) technique allows the lateral liquid phase epitaxy of Ge on insulator on Si substrates where the grown Ge crystal maintains the crystallographic orientation of the Si wafer or Si seed [9,11]. It has been shown possible to grow chip length (1 cm) GOI strips (width: 3–5 μm, thickness: 100 nm) [12] and the hybrid integration of (100), (110), and (111) orientated GOI on the same wafer [13]. The growth of (111) oriented GOI is particularly important because the

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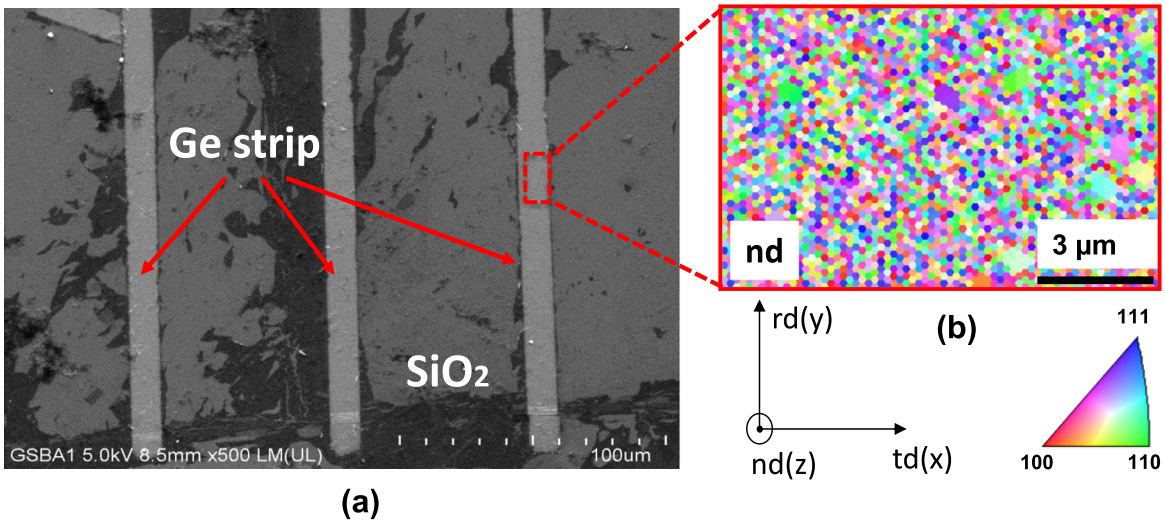

Fig. 1. (a) FESEM image of Ge microstrips (width 15 μm, length 200 μm) before annealing and (b) EBSD image in normal direction (nd). (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

maximum electron mobility in the metal-oxide-semiconductor inversion layer is achieved in the (111) plane [14]. These works trigger an idea to employ graphene as a seed layer for the growth of Ge on insulator by crystallizing the electrodeposited amorphous Ge using the rapid melting process. RMG technique is expected to be able to overcome the problem of large lattice mismatches between graphene and Ge. So far, we have also successfully reported several interesting works on the growth of silicon carbide (SiC) [15] and zinc oxide (ZnO) [16–20] on insulator by utilizing graphene as a template layer. In this work, a liquid-phase method, namely an electrochemical deposition (ECD), will be used to deposit Ge on graphene. The ECD technique seems to be a promising method to grow Ge on graphene at room temperature with high purity and good controllability of growth rate [18–20]. The same procedure of sample preparation and rapid melting process that has been applied for the formation of Si-seeded GOI structure [10–13] will be applied to crystallize the electrodeposited Ge.

2. Experimental details

The deposition of Ge on multilayer graphene (MLG)/SiO_2/Si(100) substrates (Graphene laboratories Inc., Calverton, NY, USA) was carried out in a mixture of 5% germanium(IV) chloride ($GeCl_4$) in propylene glycol ($C_3H_8O_2$) using a simple two-terminal ECD setup where graphene acted as a cathode and platinum (Pt) wire as an anode. It is worth noting that the coverage of MLG is around 95% and the properties of chemical vapor deposition grown graphene can be further found in Ref. [18]. The sample preparation including the ECD process was done at room temperature in a nitrogen-filled glove box. Both anode and cathode were connected to the external direct current (DC) power supply. The electrodeposition was operated under galvanostatic control where the current density was fixed during the deposition. The deposition was performed at fixed current density of 3.0 mA/cm^2 (potential = 3.5 V) for 75 h. The thickness of the as-deposited Ge was 400 nm.

After 75 h, the sample was removed immediately from the electrolyte and quickly rinsed with deionized (DI) water to remove any residue from the surface. The deposited Ge layer was then patterned into strips with 15 μm width and 200 μm length using conventional photolithography and wet chemical etching technique. Then, the exposed graphene was etched out by using oxygen (O_2) plasma etching in order to improve the adhesion between the capping layer and substrate's insulator. The patterned Ge strips were capped with 30 nm-thick SiN_x followed by 1 μm-thick SiO_2 layers deposited by magnetron sputtering to prevent severe agglomeration of Ge during the rapid melting process. Then, the capped Ge strips were heat treated by rapid thermal annealing process at 980 °C for 1 s. Finally, the capping layer was removed by chemical etching prior to the characterization. The as-deposited sample was cut to several pieces for the analysis which includes the characterization using Raman spectroscopy, electron back scattering diffraction (EBSD), field emission scanning electron microscopy (FESEM), and high-resolution transmission electron microscopy (HRTEM).

3. Results and discussion

First, it is worth noting that the deposition mechanism of Ge using $GeCl_4$:$C_3H_8O_2$ is considered to be the same with the deposition of Ge on Si substrate [21–23]. From the cyclic voltammogram study, it shows two reduction processes where Ge(IV) is reduced to Ge(II) prior to the deposition of Ge on substrate as summarized by Eqs. (1) and (2) [23].

$$Ge^{4+} + 2e^- \rightarrow Ge^{2+} \quad (1)$$

$$Ge^{2+} + 2e^- \rightarrow Ge \quad (2)$$

Fig. 1(a) shows the FESEM image of the patterned Ge microstrip before annealing where the morphology shows continuous and uniform strips. Based on the EDX spectra (data not shown), the deposited Ge film was found to be highly pure without any excessive contaminants such as Pt metal. Fig. 1(b) shows the color coded normal direction (ND) EBSD images of the Ge microstrip where it can be understood from the random distribution of colors that the crystal structure is amorphous.

Fig. 2 shows the Raman spectra of the as-deposited layer and the heat treated Ge microstrip. It can be seen that no significant Ge–Ge vibration mode peak was observed for the as-deposited Ge, thus confirming that the structure was amorphous. From the Raman spectra, the main peak at ~300 cm^{-1} which corresponds to Ge–Ge vibration mode was clearly observed after the rapid annealing process, confirming the crystallization of Ge. The value of full width half maximum (FWHM) of this peak was estimated to be around 3.4 cm^{-1}, which is very close to the value of the