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Influence of channel layer thickness on the stability of amorphous indium zinc oxide thin film transistors

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ABSTRACT

Amorphous indium zinc oxide (a-IZO) thin film transistors (TFTs) with different channel layer thickness were fabricated on silicon wafers by radio frequency magnetron sputtering method at room temperature. The influence of channel layer thickness on initial electrical characteristics and aging effect of a-IZO-TFTs were investigated. At the same time, the positive / negative bias stress stability of initial and 60-days-aged a-IZO-TFTs were compared. All results indicate that thin channel layer a-IZO-TFTs exhibit good anti-aging effect and bias stability.

1. Introduction

More and more attentions have been paid to the amorphous oxide semiconductor thin film transistors (AOS-TFTs) due to their advantages for advanced display technology [1,2]. a-IZO, a-IGZO and a-ZTO are the three well known AOS materials to be implemented in the TFTs as channel layer [3–6]. Although many other oxide semiconductor materials have also been explored in detail for their potential application in TFTs technology, such as SIZO [7], IZWO [8], etc., a-IZO is still the most attractive one because of its high electron mobility, room temperature processing, high uniformity, and high transparency [4,9].

In spite of promising performances of AOS-TFTs, there are still some issues to be overcome. One of the extremely important issues is the improvement of electrical stability. A lot of works have been done on this issue. Lim et al. [10] and Huan et al. [11] utilized the passivation layers to improve the bias stability of amorphous oxide thin film transistors. Cheol et al. reported the influence of device structure on the electrical stability of AOS-TFTs [12]. The improvement of photo-bias stability by the post annealing treatment was also reported [9]. As previously reported, the channel layer thickness is an important parameter to device performance, both on electrical properties [13,14] and bias stability [15–17]. But up to now, there is little report about the influence of channel layer thickness on the aging stability of a-IZO-TFTs.

In this paper, a-IZO-TFTs with different channel layer thickness were prepared by rf sputtering at room temperature. The influence of the amorphous indium zinc oxide channel layer thickness on the electrical performance of the TFT devices was investigated. The long term stability (60 days) of a-IZO-TFTs was compared with that of initial devices. The positive / negative bias stress stability were measured and compared for the initial and 60-days-aged a-IZO-TFT devices.

2. Experiment

a-IZO-TFTs with the bottom gate structure were started by thermally growing silicon dioxide (100 nm) as gate insulator layer on silicon wafers. Then, an IZO semiconductor layer was deposited by rf sputtering, using a ceramic IZO target (60 mm in diameter) in diluted O_2 ambient (Ar: O_2=3: 1). The working pressure during deposition was maintained at 0.8 Pa and the sputtering power was set at 200 W. IZO films with various thicknesses of 18 nm, 25 nm and 34 nm were obtained through the different sputtering time. The aluminum source / drain electrodes were deposited by thermal evaporation through a shadow mask (width: length=500: 100 μm). All sputtering processes were performed at room temperature without any thermal treatment. The thickness of the a-IZO channel layer was measured by a stylus profilometer (Kosaka Laboratory ET3000). The electrical characteristics were measured with Keithley 4200 in air. Then, the devices were stored in the drying cabinet (RH < 8%, ambient, 25 °C) for 60 days, and

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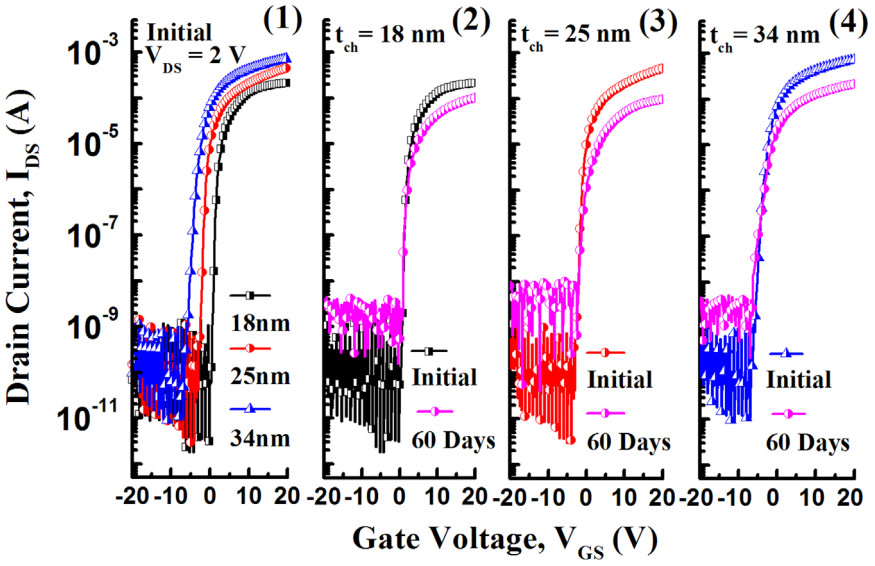

Fig. 1. (1) Initial transfer curves of a-IZO-TFTs with the different channel layer thickness; (2, 3, and 4) Transfer curves of initial and aged a-IZO-TFTs (in drying cabinet for 60 days) with the channel layer thicknesses of (2) 18 nm; (3) 25 nm; (4) 34 nm.

Table 1
Electrical characteristics of initial and aged a-IZO TFTs with different thickness of channel layer.

Active layer thickness (nm)	Threshold voltage (V)			Subthreshold Swing (V/dec)			Saturation mobility (cm^2/V s)			On/off ratio	
	Initial	After	Δ	Initial	After	Δ	Initial	After	Δ	Initial	After
18	0.92	0.87	0.05	0.28	0.54	0.26	10.79	5.16	5.63	4.9×10^6	9.5×10^4
25	−2.18	−2.40	0.22	0.44	0.71	0.27	13.77	6.67	7.10	8.1×10^6	5.7×10^4
34	−3.81	−4.3	0.49	0.67	0.99	0.32	17.25	9.39	7.86	7.8×10^6	9.1×10^4

the aging effect was evaluated through the same measurements for all devices again.

3. Results and discussion

Fig. 1 (1) shows the transfer characteristics of a-IZO-TFTs with three different channel layer thickness (t_{ch}) of 18 nm, 25 nm and 34 nm. From the figure, the on-current of a-IZO-TFTs was increased with the t_{ch} increasing, which is caused by the increased concentration of carriers that pass through source and drain. For the thicker channel layer, there are more carriers to be dragged in the channel region in the operation process [18]. The on/off current ratio is kept in the same order of magnitude ($>10^6$). To quantitatively evaluate the t_{ch} dependency of the a-IZO-TFT's performance, properties including the threshold voltages (V_{th}), the field-effect mobility (μ_{FE}), the subthreshold swing (SS) and the on/off current ratio of the a-IZO-TFTs are summarized in Table 1. The V_{th} shifts successively to more negative value as the t_{ch} increasing, e.g. the V_{th} values were decreased from 0.92 V to –3.81 V at V_{DS} of 2 V. The TFT device type changed from enhancement mode to depletion mode, which consistent with the previously reported results [13,14]. It can be commonly explained by the increasing of free carrier numbers as the t_{ch} increases, leading to the shift of V_{th} from right to left.

As shown in Table 1, the μ_{FE} increases from 10.79 cm^2/Vs to 17.25 cm^2/Vs as the t_{ch} increasing, which can be attributed to a better conductivity and an increase of carrier concentration for the thicker channel layer [14]. Meanwhile, SS can be extracted from the equation [4]:

$$SS = \frac{dV_{GS}}{d(\log I_{DS})} \quad (1)$$

According to Eq. (1), the calculated SS values are 0.28, 0.44 and 0.67 V/dec for the t_{ch} of 18, 25 and 34 nm, respectively. Apparently, the SS values show increase with respect to the t_{ch} when it ranges from 18–34 nm, as reported in previous papers [19–23]. The interfacial trap density (N_{it}) and bulk trap density (N_{bulk}) can be extracted using the following equation [14,17]:

$$N_T = N_{it} + N_{bulk} = \left(\frac{SS \log(e)}{kT/q} - 1\right)\frac{C_{ox}}{q} \quad (2)$$

Here, k is the Boltzmann constant, T is the absolute temperature, q is the charge of an electron, and C_{ox} is the capacitance of the gate insulator per unit area. We can find that the SS increased as the increasing of t_{ch}. From Eq. (2), total trap densities (N_T) in the TFTs with t_{ch} of 18, 25 and 34 nm are proportional to the SS. The N_{it} is independent on the active layer thickness [17]. But the larger thickness of films leads to the higher N_{bulk}. Therefore, N_T is proportional to the channel layer thickness, which leads to the increase of N_T as the channel layer thickness increases [14].

The transfer curves of initial and aged a-IZO-TFTs are shown in Fig. 1 (2, 3, and 4). The corresponding electrical characteristic values of V_{th}, μ_{FE}, SS and on/off current ratio are summarized in Table 1. It reveals that V_{th}, SS and μ_{FE} are also changed as t_{ch} increasing, t_{ch}-dependent tendency of electrical performance does not change after 60 days compared with that for initial devices. The on-current of 60-days-aged a-IZO-TFTs was smaller than that of the initial devices which is thought to be caused by the increasing resistivity of channel layer in the aged a-IZO-TFTs. The variation of V_{th}, SS and μ_{FE} increases with the t_{ch} (from 0.05 to 0.49, 0.26 to 0.32, and 5.63 to 7.86, respectively). It is well known