Materials Letters 133 (2014) 75–79

Contents lists available at ScienceDirect

Materials Letters

journal homepage: www.elsevier.com/locate/matlet

The effect of rapid thermal annealed seed layer on the epitaxial poly-Si thin film solar cell's structure quality and performance

Wei Li *, Sergey Varlamov, Chaowei Xue

School of Photovoltaic and Renewable Energy Engineering, University of New South Wales, Sydney, NSW 2052, Australia

ARTICLE INFO

Article history:
Received 7 May 2014
Accepted 25 June 2014
Available online 2 July 2014

Keywords:
Polycrystalline Si
Defects
Rapid thermal annealing
Epitaxy
Solar cells

ABSTRACT

Epitaxial polycrystalline Si solar cell performance is directly related to the seed layer crystal quality. In order to achieve a good crystal template for epitaxial growth, rapid-thermal annealing was used to eliminate the intragrain defects in the seed layer. Rapid thermal annealing can effectively activate the dopants and improve seed layer electronic properties. The resulted epitaxial solar cell's efficiency increases from 3.46% to 4.42% by applying rapid thermal annealing at 950 °C on the seed layer. The improved solar cell performance is related to the reduced amount of microtwins and dislocations grown from the seed layer to the epi-layer by rapid thermal annealing for the seed layer. However, higher rapid-thermal annealing temperature slightly decreases seed layer's free carrier concentration and blue response of external quantum efficiency due to the possible B diffusion from partially melted glass to the emitter.

1. Introduction

Solid-phase crystallization (SPC) of amorphous Si (a-Si) thin films is the simplest technique to obtain polycrystalline Si (poly-Si) at a relatively low temperature (600 °C). It is commonly used for poly-Si thin film solar cells fabrication [1]. However, SPC poly-Si thin films contains a large number of intragrain defects which impedes its use as the seed layer for epitaxy since the quality of the epi-layer is mostly determined by the quality of the seed layer [2]. In our previous findings, intragrain defects in the SPC seed layer can be eliminated either by rapid thermal annealing (RTA) or by line-focus diode laser annealing (DLA) [3]. DLA exhibits a superior capability to improve the structural and electronic properties of a 160 nm SPC seed layer than the RTA processing. However, the 160 nm heavily P-doped SPC seed layer is too thick to act as the emitter for the solar cell, which leads to a poor blue response. Moreover, due to the limited absorption for 808 nm, the seed layer thinner than 100 nm is shown quite limited improvement by a DLA treatment

In contrast, RTA is commonly used for dopant activation and defects removal for poly-Si thin films [4,5] and the same limitation on the film thickness as the DLA is not reported for RTA. Reducing intragrain defect density in SPC poly-Si seed layer by RTA and generating better performance of epitaxial poly-Si thin film solar cell is a motivation for this paper. Effects of RTA peak temperature on the structural and electronic qualities of the seed layer and epi-layer and the resulted solar cell performance are analyzed.

2. Experimental

The sample structure (80 nm SiN_x/80 nm a-Si with P-doping concentration at 1.7×10^{20} cm^{-3}/150 nm SiO_x) was deposited on a planar glass substrate (Schott Borofloat33) by Plasma-enhanced chemical vapor deposition (PECVD). SiN_x acts as a barrier and anti-reflection layer and SiO_x is a capping layer to protect P-doped Si from atmospheric contamination during thermal annealing. After deposition, all the samples were crystallized in a tube furnace purged with nitrogen at 600 °C. After crystallization, some of the seed layers were annealed at 850 and 950 °C for 3 min in a belt furnace heated by halogen lamps and purged with nitrogen to eliminate intragrain defects and activate the dopant [3].

Three seed layers-without RTA treatment (Sample A), with RTA treatment at 850 °C (Sample B) and with RTA treatment at 950 °C (Sample C) were chosen to deposit absorber and back surface field (BSF) layers on by E-beam evaporation at 250 °C to form a solar cell structure. These samples were then annealed at 580 °C in the nitrogen purged tube furnace for solid-phase epitaxy (SPE) [6]. SPE grown samples received another RTA processing at 950 °C for 3 min to activate dopants and to reduce the defect density. Then, high-temperature hydrogenation treatment was applied to passivate the grain boundaries [7]. These samples were metallized with

* Corresponding author.
E-mail address: weili.unsw@gmail.com (W. Li).

http://dx.doi.org/10.1016/j.matlet.2014.06.155
0167-577X/

interdigitated Al line contacts on the heavily doped layers, the emitter and BSF. All cells were in the superstrate configuration had an area of 2 cm^2 [8] and did not have any light trapping features.

The carrier concentration, electron mobility and sheet resistance of the seed layers were determined by Hall Effect measurement at room temperature. Intragrain defects in the epitaxial Si layers were analyzed by cross-sectional transmission electron microscopy (TEM) (Philips CM200 with a field emission gun). The device performance was characterized by light current–voltage ($J-V$) measurements (IV5 solar cell $I-V$ testing system from PV Measurement, Inc.) and External quantum efficiency (EQE) (QEX10 spectral response system from PV Measurements, Inc).

3. Results and discussions

Rapid thermal annealing of SPC seed layer: In Fig. 1, Sheet resistance firstly decreases from 218 Ω/sq to 183 Ω/sq as RTA peak temperature increase from room temperature to 850 °C (room temperature means without RTA processing). Meanwhile, carrier concentration increases from 5.6×10^{19} cm^{-3} to 6.5×10^{19} cm^{-3} and electron mobility increases from 64.0 to 65.4 cm^2/v s. Due to progress of the dopant activation, the higher the annealing temperature, the higher the carrier concentration and the lower the sheet resistance [9] while the higher the mobility due to the defect elimination [9]. As it was reported, trap densities can be reduced by increasing the temperature and time of the thermal annealing due to the extinction of crystal defects [10]. Additionally, it was found that RTA treatment of the SPC poly-Si films can decrease the electron spin density from 2.3×10^{17} cm^{-3} to $2.9-3.2\times10^{16}$ cm^{-3} [11]. In poly-Si, the electron spin resonance signal arises mainly from Si dangling bonds from grain boundaries [12]. Thus, RTA treatment can decrease the dangling bonds density at the grain boundaries in SPC poly-Si [11]. Based on the reasons above, RTA treatment can improve the electronic properties of the SPC seed layer.

However, when the RTA peak temperature goes above 850 °C, sheet resistance increases and the carrier concentration decreases abruptly although electron mobility increases continuously. A possible explanation might be the B contamination from the borosilicate glass. When RTA peak temperature is above the soft point of borosilicate glass (830 °C), glass is softened. In this circumstance, it is possible that boron atoms can diffuse from borosilicate glass into the Si film, even with the SiN_x diffusion barrier between the glass and Si. As reported by Inns, [13] the voids in the SiN_x barrier may allow such diffusion it may result in effective decreasing of the free carrier concentration. Therefore, the SPC seed layer shows a degraded electronic quality with the RTA peak temperature higher than 850 °C.

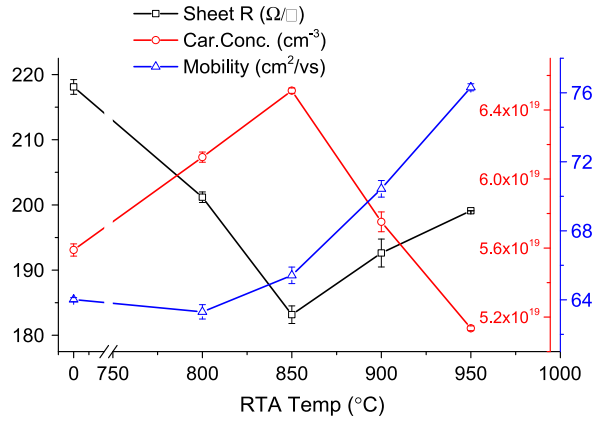

Fig. 1. Sheet resistance, carrier concentration and electron mobility of RTA treated 80 nm SPC seed layer as function of RTA plateau temperature.

Solid phase epitaxy on SPC seed layer: Fig. 2(a), (b) and (c) shows the bright-field (BF) image of the SPE grown sample A, B and C, respectively. It can be seen that grain boundaries in the SPC poly-Si seed layer propagate into the SPE grown epi-layers. The selective area electron diffraction (SAED) pattern in Fig. 2(d–f) shows corresponding to the circled region at the seed layer/epi-layer interface in Fig. 2(a–c), respectively. These SAED patterns suggest that the orientation of the seed layers and epi-layers are the same. Therefore, Fig. 2(a – c) confirms that a transfer of crystallographic information has taken place from the seed layer into the epi-layers whether the SPC seed layer is processed by RTA or not.

In Fig. 2(d) and (e), the periodic extra spots in the reciprocal lattice labeled by the red arrows are due to twins on {111} plains growing along [112] direction [14]. Satellite spots with forbidden indices 1/3(111) and 2/3(1 $\bar{1}$ 1) are Moiré patterns due to double diffraction of the electron beam by superimposing microtwins. It reveals a three-dimensional distribution of microtwins inside the grains [15]. During a SPE process, microtwins in the SPC seed layer can grow to the epi-layer. During a RTA process, reorganization of the microtwins takes place and most of the microtwins are absorbed by the larger twins. However, due to the limited RTA temperature at 850 °C, some of microtwins are still left in the SPC seed layer and can extend to the epi-layer during the SPE process. Increasing RTA temperature can effectively reduce microtwin's density in the SPC seed layer. As the RTA temperature increases to 950 °C, no periodic extra spots in the reciprocal lattice are found in the diffraction pattern in Fig. 2(f).

As shown in Fig. 2(g – i), the intragrain defects (especially dislocations) at the seed/epi-layer interface are further examined by weak beam dark-field (WBDF) TEM image taken near the Si-[$\bar{1}$10] zone axis. In a WBDF image, the dislocation line satisfying the Bragg condition shows a bright intensity peak which would be hidden in a strong-beam condition, whereas the defect-free parts of the specimen are not visible and appear dark [16]. However, in Fig. 2(g), the bright contrasts due to the twined region can strongly interfere the observation of dislocations under weak-beam condition. However, Fig. 2(g) still reveals that a high density of microtwins in the seed layer grows from seed layer to epi-layer. These microtwins are actually terminated inside the epi-layer and can introduce electronically active defects such as dislocations and high order twins [15,17] although microtwins themselves are mainly electronically inactive [18]. As shown in Fig. 2(h) and (i), SPE layers on RTA treated seed layer show much less microtwins in the seed layer and epi-layer than the one on the seed layer with SPC only. However, dislocations are still evident in the RTA treated seed layer and epi-layer. The dislocation annihilation is reported to start taking place as the annealing temperature above 1170 °C through movement unconstrained by crystallographic glide planes [19]. However, with the limitation due to the stability of the glass substrate, the maximum RTA temperature is limited to about 950 °C in this study. At this temperature, dislocations cannot be eliminated in the SPC seed layer and extend from the seed layer to epi-layer during SPE.

Dislocations that originate at the seed-epitaxy interface are also evident from Fig. 2(g – i). However, the RTA treatment can relieve the residual stress in the SPC seed layer and thus introduce fewer dislocations in the epi-layer. During the SPC process, a biaxial tensile stress usually develops in the poly-Si thin film [20]. As if the films are deposited on a stressed substrate, dislocations nucleate during film thickening [21]. RTA can effectively reduce the residual stresses in poly-Si thin films [22]. Therefore, epitaxial growth on the stress relieved RTA treated seed layer can achieve a lower dislocation density than the one on the stressed seed layer without the RTA treatment.