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Impact of the interfaces in the charge trap layer on the storage characteristics of ZrO_2/Al_2O_3 nanolaminate-based charge trap flash memory cells

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ABSTRACT

The charge trap flash memory cells incorporating high-*k* ZrO_2/Al_2O_3 nanolaminate as charge trapping layers and amorphous Al_2O_3 as tunneling and blocking layers were prepared, investigated and optimized. The interfaces between ZrO_2/Al_2O_3 nanolaminate play an important role in the charge storage characteristics. With increasing number of the interfaces in the charge trapping layer, the memory window increases first and then decreases due to electrostatic repulsion between the trapped electrons. A satisfactory retention performance was observed in the optimized cell structure, which was attributed to the deep quantum wells between the ZrO_2/Al_2O_3 nanolaminate.

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1. Introduction

Together with the feature size of conventional floating gate type nonvolatile semiconductor memory (NVSM) approaching to its scaling limitation, tremendous effort has been made to explore the low-cost, high-density and nonvolatile solid state memory devices for use in mobile electronics such as digital cameras, mobile phones and MP3 players [1]. Among the family of nonvolatile memories, the silicon-oxide–nitride-oxide–silicon (SONOS) type charge trap flash memory is a promising candidate to replace conventional floating gate flash memory due to its small size, discrete charge traps and a simple fabrication process compatible with standard complementary metal oxide semiconductor (CMOS) technology [2]. However, one problem in SONOS memory device is the small conduction band offset at the Si_3N_4/tunneling layer interface [3], which causes the electron discharging from Si_3N_4. In order to solve this problem, using high-*k* dielectrics as the charge trapping layer in SONOS structure has been reported by many researchers [4,5], due to its advantages such as higher electric field cross the tunneling layer [6] and a smaller conduction band offset (CBO) with the Si substrate [7]. In this paper, the high-*k* nanolaminate-based charge trap flash memory (CTFM) cells using the ZrO_2/Al_2O_3 nanolaminate as charge trapping layer was proposed and investigated.

2. Experimental

After cleaning the p-Si (100) substrate with a resistivity of 3–20 Ω cm, a 3 nm thick Al_2O_3 tunneling layer (TL) was deposited by the atomic layer deposition (ALD) technique. Then, the ZrO_2/Al_2O_3 nanolaminated films as the charge trapping layer (CTL) were deposited by ALD alternately using $ZrCl_4$ and $Al(CH_3)_3$ precursors, respectively. The thickness of each lamella was controlled by varying the numbers of ALD deposited cycles. In order to keep the total thickness of the ZrO_2/Al_2O_3 CTL nearly the same for different cells, the number of the lamellae in the CTL was adjusted. Subsequently, another Al_2O_3 layer of 12 nm was deposited by ALD as the blocking layer. Then the whole memory cell was rapidly thermal annealed (RTA) in N_2 ambient at 900 °C for 30 s, which was intended to simulate the influence of source/drain activating in general NVSM cell processes. Four kinds of memory cells (named as S1–S4) were fabricated by changing the thickness of each lamella in charge trapping layers, as schematically shown in Fig. 1. The Al_2O_3 layers were used as tunneling layer and blocking layer, with the thickness of about 3 nm and 12 nm, respectively, and they still remained in the amorphous state after RTA treatment. The thickness of the charge trapping layers in the samples S1, S2, S3, and S4 was measured to be about 10 nm, 10 nm, 10.5 nm and 11 nm, respectively, as shown in Fig. 1(a)–(d). Meanwhile, after RTA treatment the ZrO_2/Al_2O_3 nanolaminate became more obscure as the lamella thickness decreased. This could be ascribed to the interfacial diffusion between the ZrO_2/Al_2O_3 lamella.

3. Results and discussion

Fig. 2(a) shows the memory windows of the ZrO_2/Al_2O_3 nanolaminate-based CTFM cells. The memory cells named as S1, S2 and S4 reached their maximum memory window at ±8 V,

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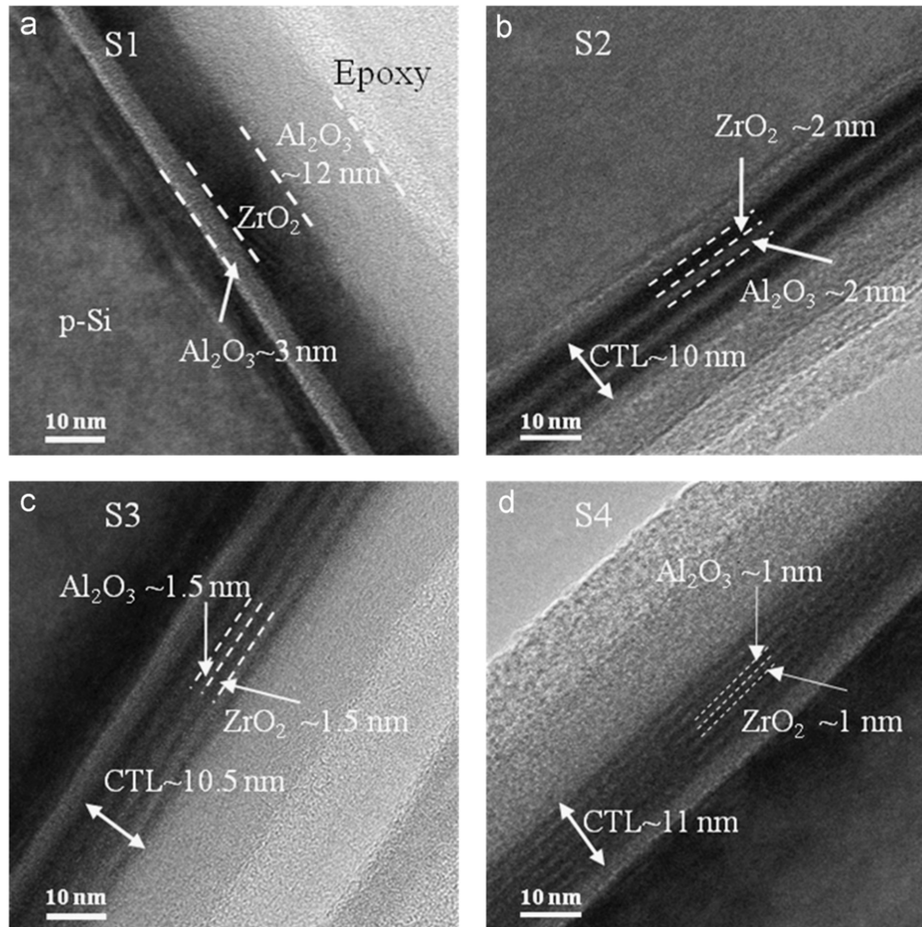

Fig. 1. Cross sectional TEM images of ZrO_2/Al_2O_3 nanolaminate-based CTFM cells: (a) a single ZrO_2 ($\sim$10 nm) film as charge trapping layer, (b) ZrO_2 (2 nm)/Al_2O_3(2 nm), (c) ZrO_2 (1.5 nm)/Al_2O_3 (1.5 nm), and (d) ZrO_2 (1 nm)/Al_2O_3 (1 nm).

$\pm$11 V and $\pm$9 V, respectively. However, no inflection point of maximum was observed using sweeping voltage up to $\pm$12 V for S3. Further increasing the sweep voltage made S3 to reach its maximum value of 6.3 V at $\pm$14 V, as shown in inset of Fig. 2(a). As described in our previous report [8], the ZrO_2 nanocrystallite-based charge trap memory without a charge trapping layer does not exhibit memory window effect. So, it is reasonable to neglect the effect of tunneling layer and blocking layer, and the interface number in the CTL plays a key role in the process of charge storage and the charges are trapped in these interfaces.

To better understand the different memory characteristics of the above four-type memory cells, one must consider two factors: the quantities of the stored charges in the charge trap layer and their stabilities. As shown in Fig. 1, the interface numbers between the ZrO_2 and Al_2O_3 lamella were increased as the thickness of the ZrO_2 and Al_2O_3 lamella was decreased because the total thickness of the nanolaminated CTL was kept constant for the four memory cells. However, the trapped electrons at the adjunct interface between the ZrO_2 and Al_2O_3 lamella will become unstable due to the increased electrostatic repulsions. A trade-off between the quantities of the stored charges and their stabilities was kept in the case of S3, whereas in S4 the quantities of the trapped charges at the interfaces in S4 became smaller due to the increased electrostatic repulsions. A schematic diagram illustrating the changes of the trapped electrons at the interfaces in S1–S4 memory cells is shown in Fig. 2(b).

Fig. 2(c) illustrates the data retention characteristics of the ZrO_2/Al_2O_3 nanolaminate-based CTFM cells. The charge loss after 10 years for these four type of memory cells can be determined to be 18.4%, 8.6%, 7.5% and 9.6%, correspondingly, by extrapolating the charge loss curve measured experimentally. The charge loss increased as the temperature of the measurement was increased. The charge loss after 10 years for S3 was extrapolated to be about 21.5% at 85 °C and 39% at 150 °C, correspondingly, as shown in Fig. 2(d).

To understand the retention performance of our memory cells, the band alignment of the ZrO_2/Al_2O_3 nanolaminate-based CTFM cells was investigated by X-ray photoelectron spectroscopy, as shown in Fig. 3. By using linear extrapolation method [9] the valence band maximums (VBM) of the p-Si substrate and the interfaces of the Al_2O_3/p-Si and ZrO_2/Al_2O_3 were determined to be 0.4 eV (E_{VBM}^{Si}), 3.6 eV ($E_{VBM}^{Al_2O_3}$) and 2.7 eV (E_{VBM}^{ZSO}), respectively, as shown in Fig. 3(a). Therefore, the valence band offsets (VBO) of the Al_2O_3/Si ($\Delta E_V^{Al_2O_3/Si}$, 3.2 eV) and the Al_2O_3/ZrO_2 ($\Delta E_V^{Al_2O_3/ZrO_2}$, $-$0.9 eV) were obtained by using the equations $\Delta E_V^{Al_2O_3/Si} = E_{VBM}^{Al_2O_3} - E_{VBM}^{Si}$ and $\Delta E_V^{Al_2O_3/ZrO_2} = E_{VBM}^{Al_2O_3} - E_{VBM}^{ZrO_2}$, respectively. To obtain the band alignment, the band gaps of Al_2O_3 and ZrO_2 were determined by the onsets of O 1*s* electron energy loss spectra collected at the interfaces of the TL/CTL, and of the CTL/BL (Fig. 3(b)). Thus, the band gaps of the TL and CTL were determined to be 7.0 eV and 4.4 eV, respectively. By using the equation $\Delta E_C^{Al_2O_3/Si} = E_g^{Al_2O_3} - E_g^{Si} - \Delta E_V^{Al_2O_3/Si}$, the values of conduction band offsets (CBO) between the TL/p-Si and TL/CTL were calculated to be 2.7 eV and 1.7 eV, respectively, where E_g^{Si} is 1.1 eV. Based on the above data, the band alignment of the memory heterostructure was established, as schematically shown in the inset of Fig. 3(b). It is expected that the large CBO value between the ZrO_2 and Al_2O_3 layers

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