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Study of SiO_2 encapsulation for aluminum and phosphorus implant activation in 4H-SiC

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ABSTRACT

SiO_2 encapsulation layer was studied for aluminum (Al) and phosphorus (P) implant activation anneal in 4H-SiC. Both Al^- and P^+ implantation were carried out at 650 °C followed by activation anneal at 1400 °C to 1500 °C. X-ray photoelectron spectroscopy (XPS), atomic force microscopy (AFM), and four-point-probe (FPP) measurements were performed to examine surface stoichiometry, roughness, and sheet resistance of the implanted SiC regions. The effect of using SiO_2 encapsulation layer for Al implant activation on the performance of 4H-SiC p-i-n diodes with both p-type active region and JTE region formed by Al implantation was also investigated. Forward and reverse characteristics including saturation current density J_0, ideality factor η, reverser leakage current density J_L and threshold breakdown voltage V_{BR} have been extracted. The results show that SiO_2 encapsulation effectively protects the SiC surface during high temperature implant activation for both Al^- and P^+.

1. Introduction

Superior material properties including electronic mobility, thermal conductivity, thermal/chemical stability and physical strength make SiC attractive for electronic applications in harsh environments where Si cannot operate. However, these material properties especially high thermal stability make the process of SiC devices more challenging, which generally requires a relatively high temperature. In various fabrication technologies, ion implantation is an important process for selective doping of SiC since the low diffusion coefficients of impurities in SiC make a diffusion process very difficult.

After ion implantation, the dopants must be thermally activated and substrate damage must be removed by high temperature annealing in the range of 1400 ~ 1700 °C [1,2]. The presence of severe surface roughening is observed on SiC implanted with Al^- or P^+ followed by high temperature annealing. A rough surface deleteriously affects the specific on-resistance and inversion layer mobility [3] of SiC power devices. To preserve surface morphology, encapsulation layers such as graphite [4] and AlN [5] have been traditionally used during implant activation. Although both cap layers have demonstrated effective protection of the SiC surface morphology, it is difficult to remove them after annealing. For example, graphite caps have to be ion-milled, plasma ashed, or oxidized, all of which damages the underlying SiC layer. It has also been reported that the use of graphite cap during high temperature activation anneal introduces trapped charges at SiC surface which lowers the inversion channel mobility in SiC MOSFETs [6]. Removing AlN requires the use of KOH which also etches SiC and thus is not well suited for SiC device fabrication.

In this paper, we investigated Al and P implant activation with SiO_2 encapsulation layer. Although SiO_2 only survives up to ~1200 °C when it is on Si, it survives higher temperatures to ~1500 °C on SiC owing to the lower vapor pressure of Si over SiC. This makes SiO_2 promising for SiC surface encapsulation during implant activation. Unlike graphite and AlN caps, there is no process difficulty associated with SiO_2 layer deposition on and removal from SiC surface. Furthermore, the process is compatible with Si-processing technology with a lower cost. All these advantages make SiO_2 capped implant annealing more suitable for SiC device fabrication.

2. Experiment

Al^- implantation (250 keV/5×10^{15} cm^{-2}) was performed on an n^--layer of 20 μm/5×10^{15} cm^{-3} on an n-type 4H-SiC substrate, while P^+ implantation (200 keV/2×10^{15} cm^{-2}) on an p-layer of 2 μm/5×10^{16} cm^{-3} on a semi-insulating 4H-SiC substrate, both at 650 °C. For p-i-n diode fabrication, Al^- implantation (100 keV/1.5×10^{15} cm^{-2}; 180 keV/2.5×10^{15} cm^{-2}; 250 keV/4×10^{15} cm^{-2}) at 650 °C was applied to form the p-type region and the JTE region. After implantation, the samples were divided into two sets, one set with surface capped by an 1 μm thick graphite layer converted from AZ photoresist by spin-coating and thermal treatment at 750 °C for 15 min in an Ar ambient, while another set with surface capped by an 1 μm thick SiO_2 layer deposited by PECVD after a two-hour thermal oxidation.

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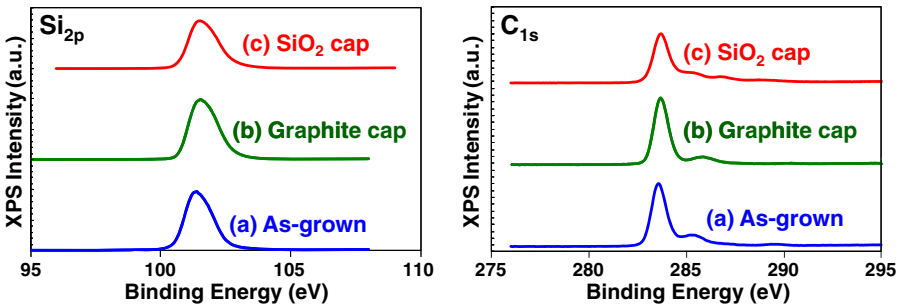

Fig. 1. XPS spectra of (a) as-grown SiC and after post-implantation annealing at 1500 °C for 30 min with (b) a graphite cap and (c) a SiO_2 cap.

Table 1
Binding energy of Si_{2p} and C_{1s}, and C/Si ratio in as-grown SiC and after annealing at 1500 °C for 30 min with a graphite cap and a SiO_2 cap.

Samples	C/Si Ratio (normalized to as-grown)	Binding Energy (eV)	
		Si_{2p}	C_{1s}
As-grown SiC	1	101.4	283.6
1500 °C, graphite cap	0.94	101.52	283.68
1500 °C, SiO_2 cap	0.96	101.51	283.68

Post-implantation annealing was performed in a pure Ar ambient. The samples with SiO_2 cap layer and graphite cap layer were annealed at 1400 ~ 1500 °C from 10 to 30 min for comparison. After annealing, the graphite cap was removed by oxidation at 1000 °C for 1 hour, and the SiO_2 cap was removed by diluted HF for 5 min. Ti/Al metal stack was used for p-type contact, and Ni for n-type contact as well as the backside cathode of the diode samples. Both n- and p-type ohmic contacts were prepared by RTA at 1000 °C for 2 min in high-purity N_2 gas.

The stoichiometry of SiC surface was examined by XPS conducted with a Kratos AXIS 165 high-performance electron spectrometer using a monochromatic Al Kα radiation. Surface roughness was characterized using AFM with a scanned area of $50 \times 50\ \mu m^2$. The sheet resistance of the implanted SiC regions was extracted by FPP measurements.

3. Results and Discussion

3.1. (a) Stoichiometry of SiC Surface

The purpose of XPS measurements is to determine whether a SiO_2 cap adversely affects the implanted SiC surface and also compare it to

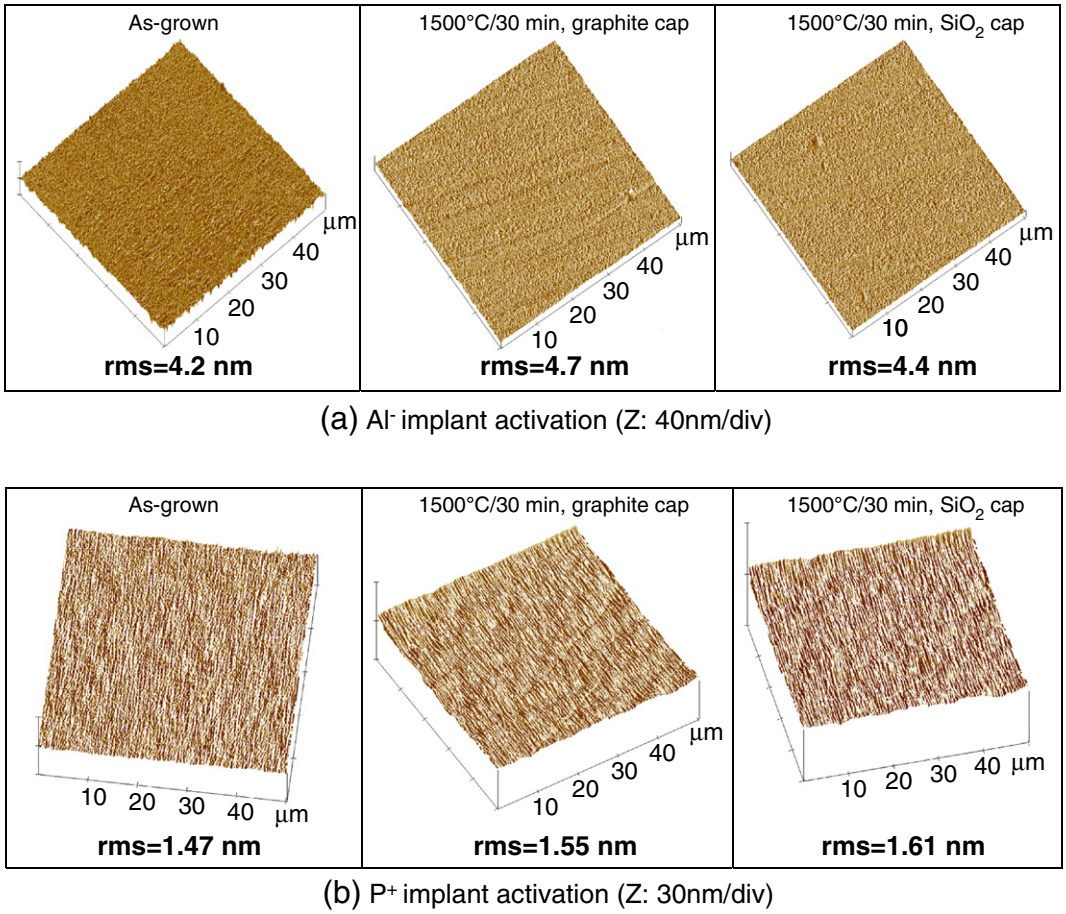

Fig. 2. AFM images of as-grown SiC and after (a) Al^- implantation and (b) P^+ implantation at 650 °C followed by high-temperature annealing at 1500 °C for 30 min with a graphite cap and a SiO_2 cap layer.