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Electron shading damage enhancement due to nonuniform in-hole etch rate in deep contact-hole process

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ABSTRACT

Degradation of gate oxides caused by etch-induced damage and inside charging of high-aspect-ratio contacts caused by process dependency on electron shading damage was investigated with Dynamic Random Access Memory (DRAM). For this, Metal-Oxide-Semiconductor (MOS) capacitors were fabricated on a 300-mm silicon wafer by using a conventional semiconductor device production process. Gate oxide degradation was evaluated by measuring the breakdown voltage shift of a MOS capacitor and the electrical fail maps of the DRAM. The metal contacts were etched under different plasma conditions, resulting in different in-hole etch rate uniformity. The results of the experiments and analytical models showed that poor etch rate uniformity inside a contact enhances gate oxide degradation due to electron shading damage.

1. Introduction

The aspect ratio generally means the ratio of depth to width of a contact or trench structure. An ever increasing aspect ratio is required for present and future semiconductor technology [1–3]. A number of problems have been identified in achieving high reliable plasma processing capable of coping with extreme design-rules. One problem is aspect ratio-dependent charging damage induced by the electron shading effect when etching metal contacts [4–8]. Previous studies on plasma damage have reported charging damage of gate oxides for samples with large antenna ratios, in particular, when the plasma touches conductive films such as the poly-silicon from the oxide layer, to form high-aspect-ratio contact holes in SiO_2 [9,10]. They also suggested that oxide degradation may result from the generation of trap or defect sites caused by the Fowler–Nordheim (FN) current due to charging on DRAM gates [11–14]. When a conductive path between the floating gate and the silicon substrate is formed by the connection of damaged sites, there is oxide breakdown, and reliability issues arise [15,16]. Therefore, it has been commonly accepted that the charging problem in micro-trench patterns is the primary source of such effects [12–14].

The main charging effect called electron shading is attributed to the presence of high-aspect-ratio patterns on the wafer. In addition, the electron shading effect is also affected by factors such as the charging time on gates and the contact area [17]. However, even if the electron shading effect is due to high-aspect-ratio metal contacts [5,17] no gate oxide degradation will occur if a good In-Hole Etch Rate Uniformity (IHERU) is maintained.

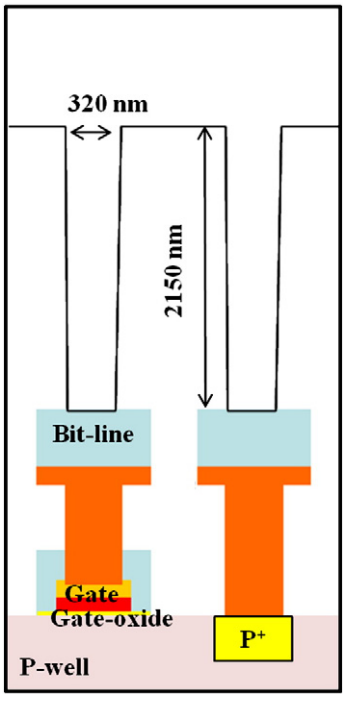

Fig. 1. Schematic diagram of the test wafer with the metal contact of DRAM.

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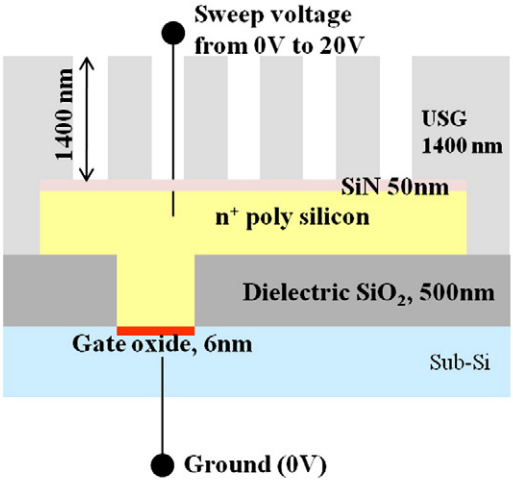

Process

Dielectric SiO_2 Depo.(500 nm) → Contact Photo / Etch → Gate Oxide Depo.(6 nm) → Poly Pad Depo. → USG Depo. (1400 nm) → Metal Contact Photo/Ecth (Plasma Damage) → USG Wet-etch → E.T.

Fig. 2. Schematic diagram of the Simple Plasma Damage Monitoring (SPDM) wafer with MOSCAP antenna. The area ratio (A_f/A_g) varies from 10 to 1200.

We examined these phenomena by etching metal contacts under plasma conditions with various IHERUs. Since a leakage current cannot be easily detected in a real device [18], a device with a large area should be used to characterize the charging damage accurately [19]. Simple Plasma Charge Damage Monitor (SPDM) [20,21] wafers with Metal-Oxide-Semiconductor Capacitor (MOSCAP) structures were used to evaluate the Plasma Process-Induced Damage (PPID) such as gate oxide breakdown and Stress-Induced Leakage Current (SILC). Consequently, degradation of the gate oxide has been evaluated by measuring the breakdown voltage and the gate current (I_g) and gate voltage(V_g) curves of SPDMs metal contacts using a plasma process under various etch conditions in a dual-frequency capacitively coupled plasma etcher.

Table 1
Etching conditions for Plasma Induced Damage (PID) evaluation.

Conditions	Etch depth (nm) (Over-etch, %)			Etch time (s)	IHERU	Over-etch
	Center	Middle	Edge			
A	2426 (13%)	2454 (14%)	2779 (29%)	250	16%	19%
B	2648 (23%)	2669 (24%)	2992 (39%)	271	16%	29%
C	2317 (12%)	2508 (16%)	2686 (25%)	250	13%	16%
D	2701 (26%)	2606 (21%)	2682 (25%)	295	1%	24%
E	2928 (36%)	2820 (31%)	2907 (35%)	319	1%	34%

2. Experiments

A test wafer was prepared based on a DRAM device with metal contacts, as shown in Fig. 1. The depth and diameter of the metal contacts were 2150 nm and 300 nm, respectively. In an attempt to characterize the PPID on the gate oxide after etching the metal contacts in the DRAM device (See Fig. 2) SPDMs with antenna MOSCAPs which have areal antennas under metal-contact modules were used. In the contact antenna modules, the thickness of the gate oxide was 6 nm, the diameter of the metal-contact was 0.25 μm, and the depth of the metal contact was 1400 nm. The antenna-to-gate area ratios (A_f/A_g) were varied from 10 to 1200, where the fixed antenna area (A_f) was $100 \times 100\ \mu m^2$. The gate oxides were, of course, completely shielded in the SPDMs. To characterize the gate oxide damage from the plasma process, SPDMs with antenna capacitors were tested by measuring the dielectric breakdown and Fowler–Nordheim (FN) tunneling current using a ramp voltage in the HP4156 system. Additionally, after curing at 430 °C for 30 min and removing the

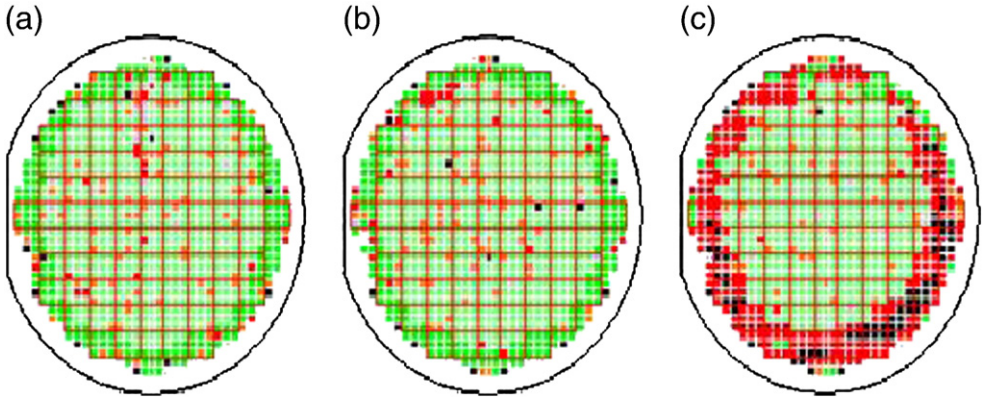

Fig. 3. Device fail maps obtained from the sample etched with the contact etching process based on etch condition (A) given in Table 1. Contact etching was performed when the RF-on time was: (a) 37 h, (b) 99 h, and (c) 150 h.