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High performance top-gated indium–zinc–oxide thin film transistors with *in-situ* formed HfO_2 gate insulator

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ABSTRACT

We report on top-gated indium–zinc–oxide (IZO) thin film transistors (TFTs) with an *in-situ* formed HfO_2 gate dielectric insulator. Building on our previous demonstration of high-performance IZO TFTs with Al_2O_3/HfO_2 gate dielectric, we now report on a one-step process, in which Hf is evaporated onto the 20 nm thick IZO channel, forming a partially oxidized HfO_x layer, without any additional insulator in-between. After annealing in air at 300 °C, the *in-situ* reaction between partially oxidized Hf and IZO forms a high quality HfO_2 gate insulator with a low interface trapped charge density N_{TC} ~ 2.3×10^{11} cm^{-2} and acceptably low gate leakage $<3 \times 10^{-7}$ A/cm^2 at gate voltage $V_G = 1$ V. The annealed TFTs with gate length $L_G = 50$ μm have high mobility ~95 $cm^2/V{\cdot}s$ (determined *via* the *Y*-function technique), high on/off ratio ~ 10^7, near-zero threshold voltage $V_T = -0.02$ V, and a subthreshold swing of 0.062 V/decade, near the theoretical limit. The on-current of our proof-of-concept TFTs is relatively low, but can be improved by reducing L_G, indicating that high-performance top-gated HfO_2-isolated IZO TFTs can be fabricated using a single-step *in-situ* dielectric formation approach.

1. Introduction

In the last ten years, amorphous oxide semiconductors have become important materials in the fabrication of high performance thin film transistors (TFTs). Such amorphous oxide semiconductors as In–Zn–O (IZO) and In–Ga–Zn–O (IGZO) have a large bandgap, relatively high mobility and can be deposited at room temperature, making them very competitive compared to amorphous Si technology [1–4]. High-performance TFTs should have a large on/off ratio, a threshold voltage close to zero, a sharp subthreshold slope and, ideally, a reasonably high on-current. While back-gated TFTs with thick insulators under the amorphous oxide channels can provide adequate performance, in order to make further progress a promising approach is to fabricate top-gated TFTs with high-quality gate insulators, which should have small interface trapped charge, high capacitance per unit area and low leakage. To fabricate high-quality gate insulators, one can reduce the gate insulator thickness, use high dielectric constant materials (such as HfO_2 or Al_2O_3) or use a multilayer gate stack [5–8].

In this paper, we improve on our previous demonstration of top-gated IZO TFTs using an *in-situ* formed dielectric layer [9] by turning to a one-step metal deposition process using Hf as the source of the *in-situ* reacted HfO_2 gate insulator. The channel material of our top-gated IZO TFTs consists of 90 wt.% In_2O_3–10 wt.% ZnO. The formation of dielectric gate insulator is based on the reaction between the metal and the IZO channel material at an intermediate temperature T ~ 200–300 °C in atmosphere. Metals (such as Hf and Al) that are thermodynamically unstable in contact with In_2O_3 will undergo solid state oxidation (in the absence of kinetic constraints) to produce a dielectric insulator layer (Al_2O_3 or HfO_2). The reaction between metal and IZO will consume oxygen from the IZO channel, leaving behind oxygen vacancies, or, in some configurations, oxidation of the metal may proceed *via* oxygen diffusion from the atmosphere. To predict which metals can be used for *in-situ* dielectric formation by reacting with IZO, one can use the free energies of oxides to find the free energy change of overall reaction [10]. For example, the free energy of the reaction between Al and In_2O_3 ($2Al + In_2O_3 = Al_2O_3 + 2In$) can be found by subtracting free formation energy of In_2O_3 from free formation energy of Al_2O_3. At 200 °C, $\Delta G^R = \Delta G^F_{Al2O3} - \Delta G^F_{In2O3} = -752.6$ kJ/mol, the negative sign indicating that without any kinetic constraints, IZO will be chemically reduced by Al to form Al_2O_3. Several metals with suitable oxides can be similarly identified including: Al ($\Delta G = -752.6$ kJ/mol), Hf ($\Delta G = -807.6$ kJ/mol), Ti ($\Delta G = -509.7$ kJ/mol), and Mg ($\Delta G = -876.1$ kJ/mol). An additional consideration is the bandgap of the resulting oxide, which must provide the needed isolation between the gate metal and the IZO channel.

Previously [9], we reported top-gated IZO TFTs with *in-situ* formed Al_2O_3 interlayer between IZO channel and HfO_2 gate insulator (those TFTs will be referred as Al-TFTs in this paper). A schematic across-sectional view of those TFTs is shown in Fig. 1(a). There is a 2–3 nm

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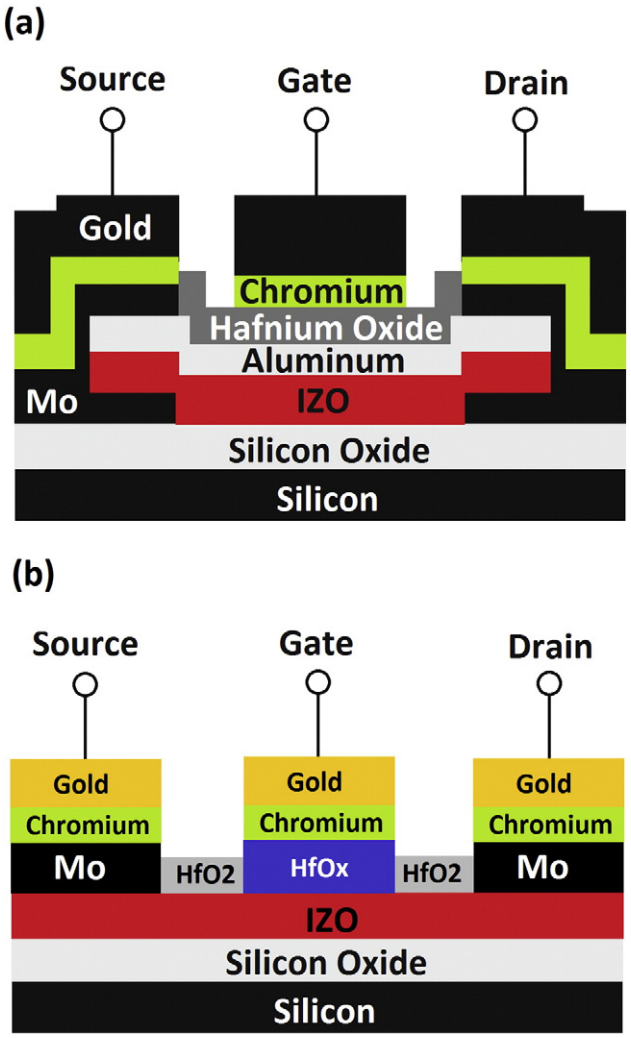

Fig. 1. (a) Schematic across-sectional view of as-deposited Al-TFTs with $W/L_G = 250/50$ μm; (b) schematic across-sectional view of as-deposited Hf-TFTs with $W/L_G = 200/50$ μm. Both types of devices are then annealed at 300 °C to form a high-quality gate dielectric of either Al_2O_3/HfO_2 (a) or HfO_2 (b) *via* metal–IZO reaction.

thick sputter-deposited Al layer between IZO and HfO_2, deposited by atomic layer deposition (ALD). This Al layer protects the IZO channel from the oxygen ion bombardment damage during ALD-deposition of HfO_2. After annealing at 300 °C, the thin Al layer will be oxidized *via* reaction with IZO, forming an Al_2O_3/HfO_2 gate stack. Those TFTs showed high mobility, high on/off ratio, and a good subthreshold slope [9]. However, a major disadvantage of using a thin layer Al between HfO_2 is the additional metal deposition step, which also necessitates addition lithographic alignment, increasing the fabrication process complexity.

In this report we present top-gated IZO TFTs by using Hf metal (those TFTs will be referred as Hf-TFTs in this paper) deposited in a single step, without any additional metal or dielectric deposition. The schematic across-sectional view of the Hf-TFTs is shown in Fig. 1(b). During the Hf evaporation, the background pressure in the deposition chamber, while low ($\sim 3 \times 10^{-3}$ Pa), is sufficient to partially oxidize the Hf. We believe that this partially oxidized material, when annealed, becomes fully oxidized HfO_2 near the IZO/HfO_x interface *via* a reaction with the IZO to produce a dielectric insulator layer that, as we shall demonstrate below, provides both low leakage and a manageable density of interface trapped charge N_{TC}. We demonstrate that these devices have promising performance, with excellent on–off ratio and sharp switching even for relatively long $L_G = 50$ μm TFTs, and small gate leakage currents.

2. Experimental procedure

Both the Al-TFTs and Hf-TFTs shown in Fig. 1, were fabricated on a silicon wafer coated with 500 nm thermally grown SiO_2. All the source, drain and gate electrodes, as well as the IZO active area, were patterned by using optical lithography and lift-off processes. In the Al-TFTs of Fig. 1(a), 10 nm of Mo was sputtered at room temperature on the source and drain area. Then 10 nm of IZO was sputtered from a 90 wt.% In_2O_3–10 wt.% ZnO target at room temperature by dc magnetron sputtering with a power density of 0.22 W/cm^2, an Ar/O_2 volume ratio of 86/64 and a dc bias of 280 V. After deposition of IZO, a 2–3 nm Al layer was deposited at room temperature by using rf-sputtering. Then, 10 nm Mo, 10 nm Cr and 70 nm Au were deposited on source and drain area using sputtering (Mo) and e-beam evaporation (Cr and Au). The HfO_2 dielectric layer was deposited by using ALD technique from a Hf $(N(CH_3)_2)_4$ precursor at 200 °C. Finally, the gate electrode (10/70 nm Cr/Au) was made using e-beam evaporation at room temperature. The width to gate length (W/L_G) ratio of the measured TFTs was 250/50 μm.

The Hf-TFTs, shown in Fig. 1(b), are also fabricated on a silicon wafer coated with 500 nm thermally grown SiO_2. Unlike the Al-TFTs, the 20 nm IZO channel was deposited directly on SiO_2 using the same magnetron sputtering process (device isolation of finished TFTs was achieved by dilute HCl etching). The source and drain contacts consisted of sputtered 50 nm Mo, followed by 10 nm Cr and 100 nm Au deposited by e-beam evaporation. After that, Hf metal was deposited on the gate area by using e-beam evaporation, forming a partially oxidized HfO_x layer due to reaction with residual oxidants in the chamber, followed by 20 nm Cr and 70 nm of Au top gate metallization. Finally, a 24 nm layer of HfO_2 was deposited using ALD as a passivation layer. The width to gate length (W/L_G) ratio of the final TFTs was 200/50 μm.

Then the capacitance was measured on a Hewlett–Packard multi-frequency LCR meter (model 4275A), whereas the current–voltage characterization used Agilent 4155C semiconductor parameter analyzer.

3. Results and discussion

The as-deposited Al-TFTs and Hf-TFTs show good TFT characteristics only after anneal, because before annealing, Al-TFTs have a thin layer of Al metal shorting the source to the drain, whereas the Hf-TFTs do not have a high-quality gate dielectric/IZO interface. After anneal at 300 °C in air, gate capacitance was measured with an LCR meter in a light-tight box using a 100 kHz ac signal on both Al-TFTs and Hf-TFTs. During capacitance measurement, source, drain and substrate Si wafer are all connected and grounded together. The gate voltage V_G was swept from negative to positive and then backward. Fig. 2 demonstrates the obtained C–V_G curves, normalized by the gate area. For the annealed Al-TFTs, when $V_G > 1$ V, capacitance reaches a maximum constant value C_{MAX} corresponding to the IZO channel in accumulation. Since we know the thickness of ALD-deposited HfO_2 to be 24 nm, the measured C_{MAX} yields a dielectric constant of HfO_2 of ~16 (with small uncertainty from the thin *in-situ* formed Al_2O_3 interlayer), which is a reasonable number for ALD-deposited HfO_2. For the Hf-TFTs, shown in Fig. 2(b), a ~ 80 nm thick layer of Hf-rich material was deposited. This layer was shown by energy-dispersive X-ray spectroscopy to be substoichiometric HfO_x, which is unsurprising, as Hf is a highly efficient oxygen getter. Taking the corresponding C_{MAX} value at $V_G = 1$ V and assuming the dielectric constant to be 16, the thickness of *in-situ* formed HfO_2 layer is ~40 nm, meaning that only part of the 80 nm partially oxidized HfO_x layer became high-quality non-leaking HfO_2 layer with a good interface in contact with IZO.

Follow-on studies will investigate the chemical change between HfO_x and IZO before and during annealing. One particularly effective tool for this would be X-ray photoelectron spectroscopy, which, as described in elsewhere [11–13], can offer insight into the composition and structure of I(G)ZO thin films. The structure of our devices – thin